



ConnectCore 95

SMARC System-on-Module

Hardware Reference Manual

Revision history—90002658

Revision	Date	Description
1P	June 2026	Initial release.

Trademarks and copyright

Digi, Digi International, and the Digi logo are trademarks or registered trademarks in the United States and other countries worldwide. All other trademarks mentioned in this document are the property of their respective owners.

© 2026 Digi International Inc. All rights reserved.

Disclaimers

Information in this document is subject to change without notice and does not represent a commitment on the part of Digi International. Digi provides this document “as is,” without warranty of any kind, expressed or implied, including, but not limited to, the implied warranties of fitness or merchantability for a particular purpose. Digi may make improvements and/or changes in this manual or in the product(s) and/or the program(s) described in this manual at any time.

Warranty

To view product warranty information, go to the following website:

www.digi.com/howtobuy/terms

Customer support

Gather support information: Before contacting Digi technical support for help, gather the following information:

- Product name and model
- Product serial number (s)
- Firmware version
- Operating system/browser (if applicable)
- Logs (from time of reported issue)
- Trace (if possible)
- Description of issue
- Steps to reproduce

Contact Digi technical support: Digi offers multiple technical support plans and service packages. Contact us at +1 952.912.3444 or visit us at www.digi.com/support.

Feedback

To provide feedback on this document, email your comments to

techcomm@diigi.com

Include the document title and part number (ConnectCore 95 SMARC SOM, 90002658 1P) in the subject line of your email.

Contents

About the ConnectCore 95 SMARC module

Features and functionality	6
Safety instructions	7
Wireless interfaces	8
WLAN IEEE 802.11a/b/g/n/ac/ax	8
Modulation and data rates	8
Data rates (Mbps)	11
RF channels	12
Transmit power	15
Antenna ports	15
Bluetooth	16

ConnectCore 95 SMARC module Microcontroller Assist (MCA)

SMARC module lines related to the MCA	18
Port A	18
Port B	19
Port C	20
Port D	21
Port F	21
Reset control	21
IOs	22
Digital IOs	23
GPIO limitation	24
MCA IRQs	24
Watchdog	24
Real-time clock	25
Power management	25
Power modes	25
SMARC_PWR_BTN# signal/Power button	27
SMARC_SLEEP# signal/Sleep button	28
CARRIER_PWR_ON and CARRIER_STBY# signals	28
FORCE_RECOV# signal	28
VIN_PWR_BAD# signal	28
MCA firmware update	28

Interfaces

SDIO	32
I2C	33

SAI	33
SPI	34
UART	34
CAN	35
USB	35
Multiplexing controlled by FORCE_RECOV#	36
Ethernet	38
PCIe	40
LVDS	41
MIPI DSI	42
MIPI CSI	43

Signals and multiplexing

Primary (top) side	45
Secondary (bottom) side	54

Module specifications

Electrical specification	64
Environmental specifications	64

About the ConnectCore 95 SMARC module

The Digi 95 SMARC redefines the SMARC® system-on-module (SOM), delivering integrated intelligence, connectivity and security — built in from the start. Based on the NXP® i.MX95 application processor, the high-performance wireless all-in-one SMARC SOM platform provides a complete, connected solution to simplify the development and management of intelligent devices.

The Digi 95 SMARC module is designed for reliability across a wide range of applications with up to six power-efficient Arm® Cortex®-A55 cores for performance, plus Cortex-M33, Cortex-M7, AI/ML NXP eIQ® Neutron NPU, 4K VPU, ISP and NXP PMICs for maximum power efficiency. The SMARC form factor offers a standardized, connector-based solution for easy integration, replacement and maintenance. It integrates memory, power management, pre-certified wireless connectivity, and advanced Digi TrustFence® device security with a complete, open-source Linux software platform based on the Yocto Project.

Features and functionality

The ConnectCore 95 SMARC module showcase the latest capabilities in embedded technologies for the standardized Digi SMTPlus (40x45) ConnectCore 95 System-on-module.

SMARC (Smart Mobility ARChitecture) is an industry standard for system-on-modules (SOMs) and single board computers (SBCs) used to develop portable devices where flexibility and scalability are relevant. The i.MX pin function available in the SMT module together with a subset of functions embedded on the SMARC module allow the integration of the ConnectCore 95 system-on-module in products designed for SMARC modules.

The following interfaces are available on the ConnectCore 95 SMARC module:

- x2 1-lane PCIe Gen 3.0
- x1 USB 3.0
- x1 USB 2.0
- x2 Gbps Ethernet ports
- x2 CAN-FD
- x1 SDIO
- x2 UART:
 - x2 two-wires (one dedicated for console port)
 - x2 four-wires (one dedicated for internal Bluetooth)
- x1 SPI
- x1 Quad SPI
- x3 I2C
- x2 SAI
- x13 General purpose I/Os
- Multimedia:

- x1 4-lane MIPI DSI/CSI
- x1 4-lane MIPI CSI
- x2 4-lane LVDS
- IEEE 802.11 a/b/g/n/ac/ax WLAN interface
- Bluetooth version 5.3

Safety instructions

- The ConnectCore 95 SMARC module cannot be guaranteed operation due to the radio link and so should not be used for interlocks in safety critical devices such as machines or automotive applications.
- The ConnectCore 95 SMARC module has not been approved for use in (this list is not exhaustive):
 - nuclear applications
 - explosive or flammable atmospheres
- There are no user serviceable components inside the ConnectCore 95 SOM. Do not modify the ConnectCore 95 in any way. Modifications may exclude the SMARC module from any warranty and can cause the ConnectCore 95 to operate outside of regulatory compliance for a given country, leading to the possible illegal operation of the radio.
- Use industry standard ESD protection when handling the ConnectCore 95 SMARC module.
- Take care while handling to avoid electrical damage to the PCB and components.
- Do not expose ConnectCore 95 SMARC module to water or moisture.
- Use this product with the antennas specified in the ConnectCore 95 SOM user guides.
- The end user must be told how to remove power from the ConnectCore 95 SMARC module or to locate the antennas 20 cm from humans or animals.

Wireless interfaces

The ConnectCore 95 SMARC module combines a wireless local area network (WLAN) and Bluetooth dual solution to support IEEE802.11 a/b/g/n/ac/ax WLAN standards and Bluetooth 5.3, enabling seamless integration of WLAN/Bluetooth and Low Energy technology. Digi also offers a non-wireless variant of the ConnectCore 95 SMARC module.

The following sections include specifications for the wireless interfaces available on the ConnectCore 95 SMARC module.

WLAN IEEE 802.11a/b/g/n/ac/ax

The following sections specify the performance of the WLAN IEEE 802.11a/b/g/n/ac/ax interface on the ConnectCore 95 SMARC module.

Modulation and data rates

The following tables list modulation values for the ConnectCore 95 SMARC module, which supports the following WLAN standards:

Mode	Modulation & coding	Rate
802.11b	DBPSK	1 Mbps
	DQPSK	2 Mbps
	CCK	5.5 Mbps
	CCK	11 Mbps

Mode	Modulation & coding	Rate
802.11ga	BPSK-1/2	6 Mbps
	BPSK-3/4	9 Mbps
	QPSK-1/2	12 Mbps
	QPSK-3/4	18 Mbps
	16QAM-1/2	24 Mbps
	16QAM-3/4	36 Mbps
	64QAM-2/3	48 Mbps
	64QAM-3/4	54 Mbps
802.11n	BPSK-1/2	MCS0
	QPSK-1/2	MCS1
	QPSK-3/4	MCS2
	16QAM-1/2	MCS3
	16QAM-3/4	MCS4
	64QAM-2/3	MCS5
	64QAM-3/4	MCS6
	64QAM-5/6	MCS7

Mode	Modulation & coding	Rate
802.11ac	BPSK-1/2	MCS0
	QPSK-1/2	MCS1
	QPSK-3/4	MCS2
	16QAM-1/2	MCS3
	16QAM-3/4	MCS4
	64QAM-2/3	MCS5
	64QAM-3/4	MCS6
	64QAM-5/6	MCS7
	256QAM-3/4	MCS8
	256QAM-5/6	MCS9
802.11ax	BPSK-1/2	MCS0
	QPSK-1/2	MCS1
	QPSK-3/4	MCS2
	16QAM-1/2	MCS3
	16QAM-3/4	MCS4
	64QAM-2/3	MCS5
	64QAM-3/4	MCS6
	64QAM-5/6	MCS7
	256QAM-3/4	MCS8
	256QAM-5/6	MCS9
	1024QAM-3/4	MCS10
	1024QAM-5/6	MCS11

Data rates (Mbps)

Standard	Bandwidth	Guard interval	Data rate (Mbps)							
			1 Mbps	11 Mbps	6 Mbps	54 Mbps	MCS0	MCS7	MCS9	MCS11
802.11b/g/a/n/ac	20 MHz	0.8 us	1	11	6	54	6.5	65		
		0.4 us	1	11	6	54	7.2	72.2		
	40 MHz	0.8 us					13.5	135	180	
		0.4 us					15	150	200	
	80 MHz	0.8 us					29.3	292.5	390	
		0.4 us					32.5	325	433.3	
802.11ax	20 MHz	3.2 us					7.3	73.1	97.5	121.9
		1.6 us					8.1	81.3	108.3	135.4
		0.8 us					8.6	86	114.7	143.4
	40 MHz	3.2 us					14.6	146.3	195	243.8
		1.6 us					16.3	162.5	216.7	270.8
		0.8 us					17.2	172.1	229.4	286.8
	80 MHz	3.2 us					30.6	306.3	408.3	510.4
		1.6 us					34	340.3	453.7	567.1
		0.8 us					36	360.3	480.4	600.5

RF channels

The ConnectCore 95 SMARC module supports the following frequency bands:

RF band	Ch. BW	Ch. spacing	Channel number (Center freq. MHz)
2.4 GHz	20 MHz	5 MHz	1(2412), 2(2417), 3(2422), 4(2427), 5(2432), 6(2437), 7(2442), 8(2447), 9(2452), 10(2457), 11(2462), 12(2467), 13(2472), 14(2484)
	40 MHz	5 MHz	3(2422), 11(2462)
5 GHz	20 MHz	20 MHz	36(5180), 40(5200), 44(5220), 48(5240), 52(5260), 56(5280), 60(5300), 64(5320), 100(5500), 104(5520), 108(5540), 112(5560), 116(5580), 120(5600), 124(5620), 128(5640), 132(5660), 136(5680), 140(5700), 144(5720), 149(5745), 153(5765), 157(5785), 161(5805), 165(5825)
	40 MHz	40 MHz	38(5190), 46(5230), 54(5270), 62(5310), 102(5510), 110(5550), 118(5590), 126(5630), 134(5670), 142(5710), 151(5755), 159(5795)
	80 MHz	80 MHz	42(5210), 58(5290), 106(5530), 122(5610), 138(5690), 155(5775)

Note Dependent upon regulatory bodies.

2.4 GHz

2.4 GHz band channel #	Center frequency (MHz)	EUROPE (ETSI)	NORTH AMERICA (FCC)	JAPAN
1	2412	✓	✓	✓
2	2417	✓	✓	✓
3	2422	✓	✓	✓
4	2427	✓	✓	✓

2.4 GHz band channel #	Center frequency (MHz)	EUROPE (ETSI)	NORTH AMERICA (FCC)	JAPAN
5	2432	✓	✓	✓
6	2437	✓	✓	✓
7	2442	✓	✓	✓
8	2447	✓	✓	✓
9	2452	✓	✓	✓
10	2457	✓	✓	✓
11	2462	✓	✓	✓
12	2467	✓	No	✓
13	2472	✓	No	✓
14	2484	No	No	802.11b only

5 GHz

5 GHz band channel #	Center frequency (MHz)	EUROPE (ETSI)	NORTH AMERICA (FCC)	JAPAN
36	5180	Indoors	✓	✓
40	5200	Indoors	✓	✓
44	5220	Indoors	✓	✓
48	5240	Indoors	✓	✓
52	5260	Indoors / DFS / TPC	DFS	DFS / TPC
56	5280	Indoors / DFS / TPC	DFS	DFS / TPC
60	5300	Indoors / DFS / TPC	DFS	DFS / TPC
64	5320	Indoors / DFS / TPC	DFS	DFS / TPC

5 GHz band channel #	Center frequency (MHz)	EUROPE (ETSI)	NORTH AMERICA (FCC)	JAPAN
100	5500	DFS / TPC	DFS	DFS / TPC
104	5520	DFS / TPC	DFS	DFS / TPC
108	5540	DFS / TPC	DFS	DFS / TPC
112	5560	DFS / TPC	DFS	DFS / TPC
116	5580	DFS / TPC	DFS	DFS / TPC
120	5600	DFS / TPC	DFS	DFS / TPC
124	5620	DFS / TPC	DFS	DFS / TPC
128	5640	DFS / TPC	DFS	DFS / TPC
132	5660	DFS / TPC	DFS	DFS / TPC
136	5680	DFS / TPC	DFS	DFS / TPC
140	5700	DFS / TPC	DFS	DFS / TPC
149	5745	SRD	✓	No Access
153	5765	SRD	✓	No Access
157	5785	SRD	✓	No Access
161	5805	SRD	✓	No Access
165	5825	SRD	✓	No Access

Note

DFS = Dynamic Frequency Selection

TPC = Transmit Power Control

SRD = Short Range Devices 25 mW max power

Transmit power

The following table lists nominal transmit power values for the ConnectCore 95 SMARC module based on Murata specification.

RF band	Standard	Nominal Output power (dBm)
2.4 GHz	802.11b	18 (1 Mbps) - 18 (11 Mbps)
	802.11g	17 (6 Mbps) - 17 (54 Mbps)
	802.11n	16 (MCS0, HT20) - 16 (MCS7, HT20)
	802.11ax	14 (MCS0, HE20) - 12 (MCS11, HE20)
5 GHz	802.11a	16 (6 Mbps) - 16 (54 Mbps)
	802.11n	14 (MCS0, HT20) - 14 (MCS7, HT20) 14 (MCS0, HT40) - 14 (MCS7, HT40)
	802.11ac	14 (MCS0, VHT20) - 10 (MCS8, VHT20) 14 (MCS0, VHT40) - 10 (MCS9, VHT40) 14 (MCS0, VHT80) - 10 (MCS9, VHT80)
	802.11ax	12 (MCS0, HE20) - 9 MCS11 (HE20) 12 (MCS0, HE40) - 9 (MCS11, HE40) 12 (MCS0, HE80) - 9 (MCS11, HE80)
6 GHz	802.11a	12 (6 Mbps) - 12 (24 Mbps)
	802.11ax	11 (MCS0, HE20) - 9 (MCS11, HE20) 11 (MCS0, HE40) - 9 (MCS11, HE40) 11 (MCS0, HE80) - 9 (MCS11, HE80)

Note Output power values are subject to change.

Antenna ports

The ConnectCore 95 SMARC module has one antenna port on the module via a dedicated U.FL connector. The antenna port supports WLAN and Bluetooth functionality.

Bluetooth

The ConnectCore 95 SMARC module supports both Bluetooth and Bluetooth Low Energy protocols:

- Bluetooth 5.3 with all Bluetooth 4.2 optional features. Bluetooth class 1 and class 2 transmitter operation.
- Integrated WLAN-Bluetooth coexistence.

ConnectCore 95 SMARC module Microcontroller Assist (MCA)

The Microcontroller Assist, or MCA, is a microcontroller that is deeply integrated into the design of the ConnectCore 95 SMARC module. It assists the i.MX95 processor with advanced operations related to power management, security, and system reliability. It also assist the ConnectCore 95 SMARC module to cope with some SMARC specification functionality.

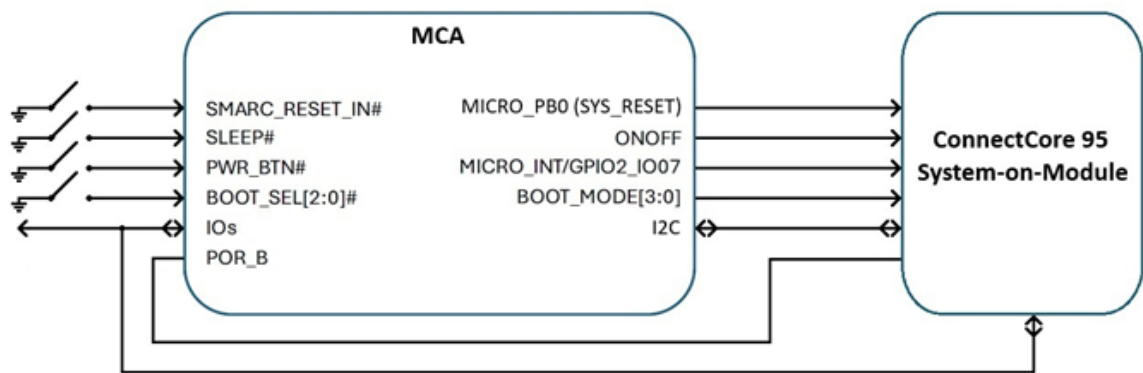
The functionality provided by the MCA includes:

- Advanced power management such as power and sleep buttons and wake up sources.
- Peripheral extensions such as GPIO, RTC, and watchdog.
- Handling of some SMARC specific functionality such as:
 - CARRIER_PWR_ON, CARRIER_STBY#
 - FORCE_RECOV#
 - VIN_PWR_BAD#
 - Boot select translation
- Providing to users through generic GPIOs the handling of some SMARC specific functionality such as:
 - BATLOW#
 - CHARGER_PRSTN#
 - CHARGING#
 - LID#
 - RESET_OUT#
 - TEST#

The MCA and the i.MX95 are connected through an I2C interface and an interrupt line. The microcontroller provides up to 29 general purpose IOs that can be configured with different modes to provide functionality such as digital input/output.

The i.MX95 can update the MCA firmware over the I2C bus. See the [MCA software documentation](#) for additional information about this process.

The diagram below shows the interconnection between the MCA and the ConnectCore 95 SMARC module:



SMARC module lines related to the MCA

Port A

MCA Port A pin	SMARC CONNECTOR NAME	Function	Pin direction	Definition
0	SMARC_PWR_BTN#	CC95 SMARC Power Button	Input	SMARC Specific
1	SMARC_RESET_OUT#	MCA_IO11	Bidirectional	General purpose Input/Output
2	SMARC_GPIO1/CAM1_PWR#	MCA_IO1	Bidirectional	General purpose Input/Output
3	SMARC_GPIO0/CAM0_PWR#	MCA_IO0	Bidirectional	General purpose Input/Output
4	SMARC_CHARGING#	MCA_IO12	Bidirectional	General purpose Input/Output
5	SMARC_CHARGER_PRSENT#	MCA_IO8	Bidirectional	General purpose Input/Output
6	SMARC_CARRIER_STBY#	Asserted when CC95 SMARC is in standby	Output	SMARC Specific
7	SMARC_CARRIER_PWR_ON	Asserted when CC95 SMARC is on	Output	SMARC Specific
8	SMARC_FORCE_RECOV#	Forces USB recovery	Input	SMARC Specific
9	SMARC_BATLOW#	MCA_IO13	Bidirectional	General purpose Input/Output
10	SMARC_TEST#	MCA_IO14	Bidirectional	General purpose

MCA Port A pin	SMARC CONNECTOR NAME	Function	Pin direction	Definition
				Input/Output
11	SMARC_GPIO9	MCA_IO15	Bidirectional	General purpose Input/Output
12	SMARC_ESPI_RESET#	MCA_IO16	Bidirectional	General purpose Input/Output
13	SWDIO/SMARC_PCIE_C_RST#	SWDIO/MCA_IO17	Bidirectional	General purpose Input/Output
14	SWCLK/SMARC_GPIO7	SWCLK/MCA_IO18	Bidirectional	General purpose Input/Output
15	SMARC_GPIO11	MCA_IO5	Bidirectional	General purpose Input/Output

Port B

MCA Port B pin	SMARC CONNECTOR NAME	Function	Pin direction	Definition
0	NA	SYSRESET	Input	CC95 Internal
1	SMARC_PCIE_B_RST#	MCA_IO10	Bidirectional	General purpose Input/Output
2	SMARC_LCD1_BKLT_EN	MCA_IO19	Bidirectional	General purpose Input/Output
3	SMARC_LCD1_VDD_EN	MCA_IO20	Bidirectional	General purpose Input/Output
4	SMARC_LCD0_BKLT_EN	MCA_IO21	Bidirectional	General purpose Input/Output
5	SMARC_LCD0_VDD_EN	MCA_IO22	Bidirectional	General purpose Input/Output
6	NA	INT_I2C8_SCL	Input	CC95 Internal
7	NA	INT_I2C8_SDA	Bidirectional	CC95 Internal
8	SMARC_PCIE_WAKE	MCA_IO23	Bidirectional	General purpose Input/Output
9	SMARC_SDIO_WP#	MCA_IO24	Bidirectional	General purpose Input/Output
10	SMARC_PCIE_A_RST#	MCA_IO25	Bidirectional	General purpose Input/Output

MCA Port B pin	SMARC CONNECTOR NAME	Function	Pin direction	Definition
11	SMARC_GPIO4	MCA_IO4	Bidirectional	General purpose Input/Output
12	SMARC_GPIO3	MCA_IO3	Bidirectional	General purpose Input/Output
13	SMARC_GPIO2	MCA_IO2	Bidirectional	General purpose Input/Output
14	SMARC_SLEEP#	CC95 SMARC Sleep Button	Input	SMARC Specific
15	SMARC_VIN_PWR_BAD#	CC95 SMARC Input voltage detection line	Input	SMARC Specific

Port C

MCA Port C pin	SMARC CONNECTOR NAME	Function	Pin direction	Definition
0	NA	PMIC_ON	Input	CC95 Internal
1	NA	ENET_INT_N at MCA_IO26	Bidirectional	CC95 Internal
2	NA	MICRO_INT: MCA interrupts the CPU	Output	CC95 Internal
3	NA	EXT_RTC_INT_N at MCA_IO27	Bidirectional	CC95 Internal
4	NA	TEMP_ALERT at MCA_IO28	Bidirectional	CC95 Internal
5	NA	ONOFF: Power on/off the PMIC	Output	CC95 Internal
6	SMARC_BOOT_SEL0#	BOOT_SEL0	Input	SMARC Specific
7	SMARC_BOOT_SEL1#	BOOT_SEL1	Input	SMARC Specific
8	SMARC_BOOT_SEL2#	BOOT_SEL2	Input	SMARC Specific
9	NA	BOOT_MODE0	Output	CC95 Internal
10	NA	BOOT_MODE1	Output	CC95 Internal
11	NA	BOOT_MODE2	Output	CC95 Internal
12	NA	BOOT_MODE3	Output	CC95 Internal

MCA Port C pin	SMARC CONNECTOR NAME	Function	Pin direction	Definition
13	SMARC_LID#	MCA_IO9	Bidirectional	General purpose Input/Output
14	NA	OSC32	Input	CC95 Internal
15	NA	OSC32	Output	CC95 Internal

Port D

MCA Port D pin	SMARC CONNECTOR NAME	Function	Pin direction	Definition
2	NA	POR_B	Bidirectional	CC95 Internal

Port F

MCA Port F pin	SMARC CONNECTOR NAME	Function	Pin direction	Definition
0	NA	Not Used	NA	CC95 Internal
1	SMARC_GPIO12	MCA_IO6	Bidirectional	General purpose Input/Output
2	SMARC_RESET_IN#	Resets CC95 SMARC module	Input	SMARC Specific
3	SMARC_GPIO13	MCA_IO7	Bidirectional	General purpose Input/Output

Reset control

Asserting and de-asserting the SMARC_RESET_IN# line resets the module regardless the operating mode of the system. Then, the microcontroller executes the programmed firmware.

The MCA, in cooperation with the PMIC, controls the reset line of the i.MX95 processor (POR_B).

The SMARC_RESET_IN# pin is the main reset input of the ConnectCore 95 SMARC module. This pin is a pseudo open-drain with an internal pull up. Asserting the SMARC_RESET_IN# line low sets the MCA into reset state, and it remains in this state until the line is de-asserted.

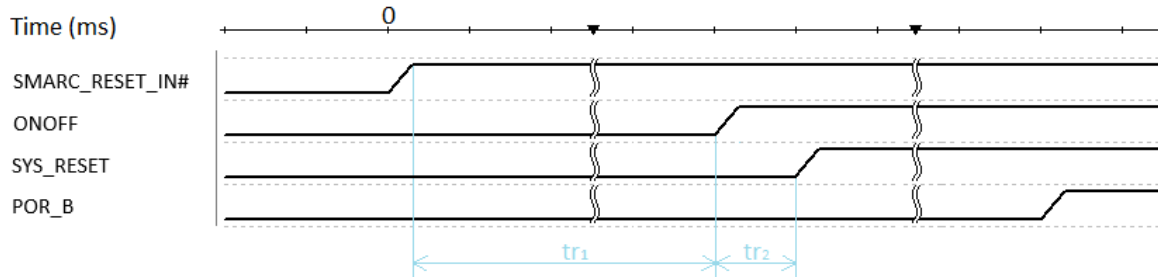
During system initialization, the MCA performs the following actions:

- Asserts the ON_OFF line low for a configurable number of milliseconds (0-255 ms with a default value of 50ms), keeping the CC95 module switched-off.
- Asserts the ON_OFF line high to power the system on (assuming it was asserted low before).
- Keeps SYS_RESET asserted low for a configurable number of milliseconds.
- Releases the SYS_RESET line to start the execution of the firmware on the i.MX95 processor.

Note The POR_B line is controlled by the PMIC. The PMIC won't release this line until it is switched on and the entire starting sequence is finished (a few ms after the latest regulator is turned on). This means that even if the MCA releases the reset line of the module (SYS_RESET), the CPU won't go out of reset until the PMIC ends its own power-up sequence.

The following time diagram represents the reset sequence. You can configure the reset timing. Default values are as follows:

- tr1: 50 ms
- tr2: 1 ms



See the [MCA software documentation](#) for additional information on the configuration of the MCA.

IOs

The ConnectCore 95 SMARC module MCA provides up to twenty nine configurable IOs.

All IOs have digital I/O capabilities and are IRQ capable.

The following table lists all available MCA IOs and their connection to the SMARC connector pins:

MCA_IO	SMARC CONNECTOR NAME	SMARC CONNECTOR PAD	ConnectCore 95 SMARC SOM USAGE
0	SMARC_GPIO0	P108	
1	SMARC_GPIO1	P109	
2	SMARC_GPIO2	P110	
3	SMARC_GPIO3	P111	
4	SMARC_GPIO4	P112	
5	SMARC_GPIO11	P119	
6	SMARC_GPIO12	S142	
7	SMARC_GPIO13	S123	
8	SMARC_CHARGER_PRSENT#	S152	
9	SMARC_LID#	S148	

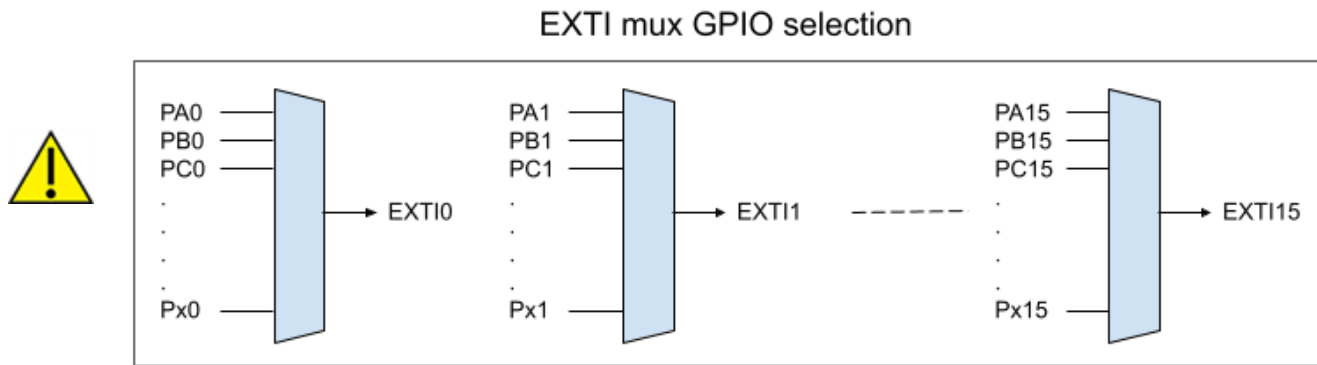
MCA_IO	SMARC CONNECTOR NAME	SMARC CONNECTOR PAD	ConnectCore 95 SMARC SOM USAGE
10	SMARC_PCIE_B_RST#	S76	
11	SMARC_RESET_OUT#	P126	
12	SMARC_CHARGING#	S151	
13	SMARC_BATLOW#	S156	
14	SMARC_TEST#	S157	
15	SMARC_GPIO9	P117	
16	SMARC_ESPI_RESET#	S58	
17	SMARC_PCIE_C_RST#	S77	
18	SMARC_GPIO7	S4	
19	SMARC_LCD1_BKLT_EN	S107	
20	SMARC_LCD1_VDD_EN	S116	
21	SMARC_LCD0_BKLT_EN	S127	
22	SMARC_LCD0_VDD_EN	S133	
23	SMARC_PCIE_WAKE	S146	
24	SMARC_SDIO_WP#	P33	
25	SMARC_PCIE_A_RST#	P75	
26	NA	NA	ENET_INT_N
27	NA	NA	EXT_RTC_INT_N
28	NA	NA	TEMP_ALERT

Digital IOs

All MCA IOs can be configured as digital inputs/outputs, which are powered from the 1V8_MICRO power rail. The digital outputs preserve the output value set in all operating modes, except in power off mode where the IOs are reconfigured to high impedance state to preserve power.

GPIO limitation

The STM32U031 SoC has a limitation in the number of GPIOs that can be used as interrupt lines. The Extended Interrupt and Event Controller (EXTI) can only handle up to 16 GPIO lines working as interrupt (EXTI0..EXTI15). The multiplexers work as shown in the following figure:



This means that if pin 1 of a given port (for instance, PB1) has been selected to work as interrupt, pin 1 of any other GPIO port cannot simultaneously work as interrupt.

When designing your hardware, avoid using the same GPIO numbers as interrupt lines of two or more peripherals.

MCA IRQs

You can configure the MCA IOs as interrupt inputs, using the MCA software to configure them as edge interrupts (rising, falling, or both) or as level interrupts (high level or low level). The firmware provides a configurable debounce filter for each GPIO that improves noise immunity and filters rebounds on push buttons. When one or more MCA IRQs are activated, the MCA interrupts the main processor through the corresponding IRQ line, signaling the active IRQs in the IRQ status registers. The IRQ inputs can wake the system from any low power mode (suspend or power off).

See the [MCA software documentation](#) for additional information about how to configure and access the MCA IRQ lines.

Watchdog

The MCA implements a watchdog timer in its firmware. The MCA watchdog resets the system, or only the i.MX95 CPU, if the software running on the main processor fails to execute properly and does not reset the watchdog timer on time.

The main features of the MCA watchdog include:

- Configurable timeout between 1 and 255 seconds.
- Configurable to generate interrupt or system reset.
- Configurable to generate full-system reset (including the MCA itself) or CPU-only reset. Full system reset can include a PMIC off/on, depending on the device configuration.

See the [MCA software documentation](#) for additional information about how to configure and access the watchdog timer.

Real-time clock

The MCA implements a Real-Time Clock (RTC) in its firmware. The i.MX95 CPU internal RTCs are disabled by default because the MCA RTC is preferred due to its superior power consumption efficiency. To preserve the date during power-off, you must connect a coin cell battery to VDD_RTC. The main features of the MCA RTC include:

- Date/time registers to keep the system time (backed up by the coin cell battery).
- Programmable alarm to generate an interrupt. This alarm can be used to wake the system from low power modes (suspend and power off).

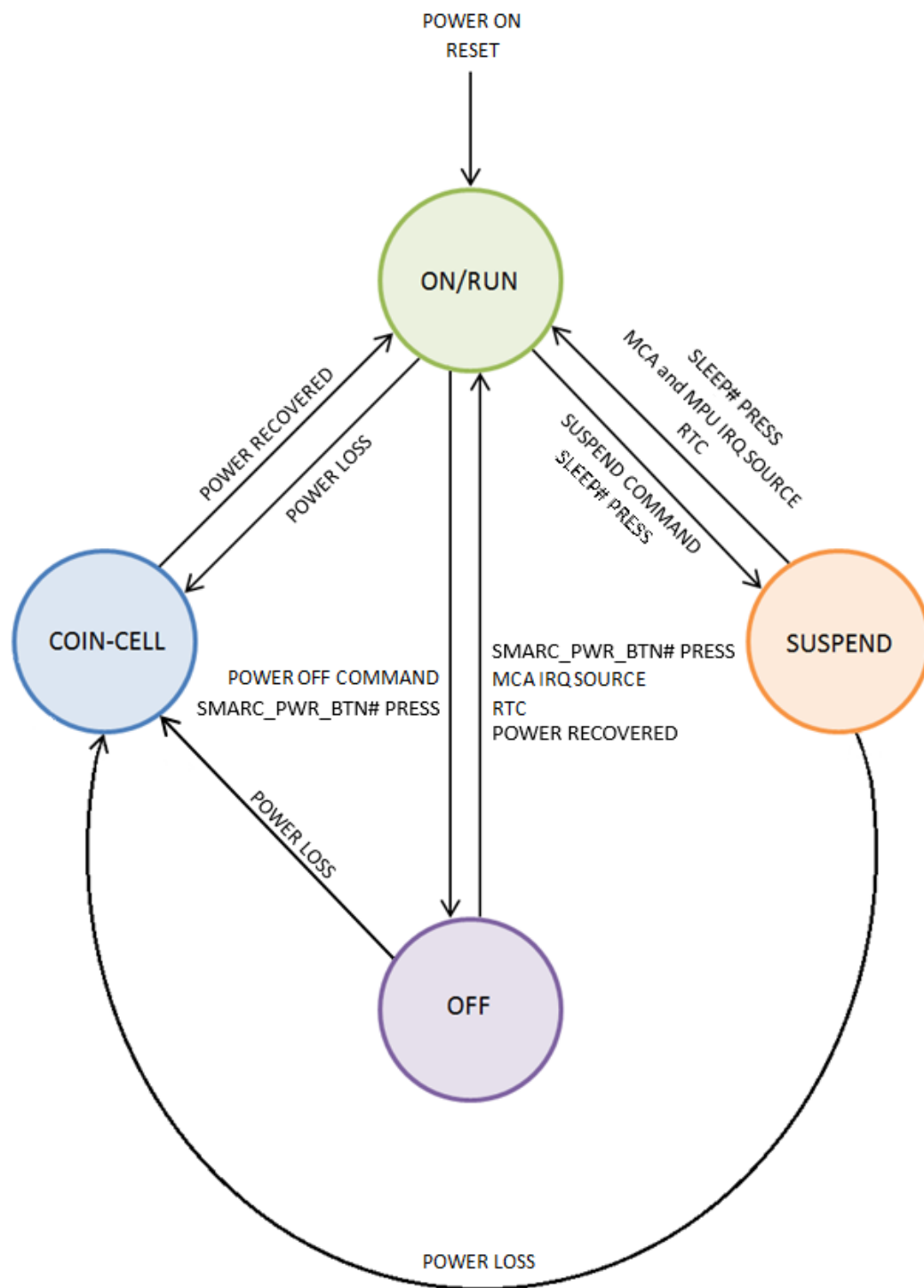
See the [MCA software documentation](#) for additional information about how to configure and access the RTC.

Power management

The MCA plays a key role in the power management activities of the ConnectCore 95 SMARC module. In cooperation with the i.MX95 processor, the MCA controls the power states of the PMIC and provides multiple wake up sources to transition between power modes. It also allocates dedicated signals to capture power events and indicate the system power state, allowing to control external power sources and indicators.

Power modes

The module provides four different power operating modes: ON/RUN, OFF, SUSPEND, and COIN-CELL. The following figure shows the state diagram and the events to switch between states.



ON/RUN mode

The module enters the ON state after a power-on or system-reset event.

In this mode, the PMIC is running at full power so all voltage regulators are generating the nominal voltage for this mode. The CPU reset line is de-asserted and the processor is running at normal speed, performing DVFS if the system was configured to do so. In this state, the ONOFF line is asserted high, indicating that the module is ON.

Note that the specific state of the regulators (on/off) and the voltage in this mode are controlled by the firmware running on the i.MX95 processor. The PMIC starts with the default settings configured on the OTP area, but once the software takes control it applies the specific configuration implemented in the firmware.

SUSPEND mode

The suspend mode (also known as suspend-to-RAM mode) is the low-power mode that allows the module to preserve RAM content. When the module enters SUSPEND, the following actions take place:

- The processor goes into low power, disabling as much functionality as possible and keeping active only the peripherals configured to wake the system from SUSPEND.
- The DDR memory is set to self-refresh mode to preserve its contents while reducing power consumption.
- The PMIC goes into standby mode, configuring the regulators in a specific mode (on, off, with a different voltage compared to ON state).
- The MCA goes into sleep mode, keeping active the peripherals that always run in low power modes (like the RTC) and those configured to wake up the system (such as IRQs and power IO). MCA GPIOs configured as outputs also keep their value.

OFF mode

The module enters OFF mode after a power-off event. In this mode:

- The PMIC is set to the OFF state.
- The ONOFF line is asserted low, indicating that the module is in OFF state.
- The MCA goes into sleep mode, keeping active the peripherals that always run in low-power modes (like the RTC) and those configured to wake up the system (such as IRQs and power IO).

COIN-CELL mode

The MCA does also support the coin-cell mode. This operating mode is intended to keep a minimal set of functionalities alive (typically RTC) when the main supply voltage, VDD_IN, is removed. In order to support this operating mode, a coin cell battery or supercapacitor must be connected to VDD_RTC.

SMARC_PWR_BTN# signal/Power button

The MCA provides a signal (SMARC_PWR_BTN#) to detect external events that trigger a transition between the ON and OFF modes as described in the [Power modes](#) section. The pin has wake-up interrupt/event capabilities, it is active low, and it provides an internal pull-up. This signal is ideal for connecting a power button or the output of a peripheral that controls the power state of the module and its transitions.

The firmware provides a configurable debounce filter to improve noise immunity and filter rebounds on push buttons. When the SMARC_PWR_BTN# signal is asserted low, the system triggers the power

off interrupt, to tell the host processor to start a transition to OFF state. If the low-pulse duration is long enough (time-configurable by the user), the MCA will automatically set the OFF state.

SMARC_SLEEP# signal/Sleep button

The MCA provides a signal (SMARC_SLEEP#) to detect external events that trigger a transition between the ON and SUSPEND modes as described in the [Power modes](#) section. The pin has wake-up interrupt/event capabilities, it is active low, and it provides an internal pull-up.

The firmware provides a configurable debounce filter to improve noise immunity and filter rebounds on push buttons. When the SMARC_SLEEP# signal is asserted low, the system will trigger an interrupt that, commonly, indicates the host processor that the system should enter suspend state.

See the [MCA software documentation](#) for more information on the SLEEP# signal.

CARRIER_PWR_ON and CARRIER_STBY# signals

The MCA sets these signals level according to the system current power state:

- CARRIER_PWR_ON will be high while the system is ON (including standby mode), and will go low when the system go to poweroff mode.
- CARRIER_STBY# signal will be high while the system is ON, and will go low when the system go to standby mode.

FORCE_RECOV# signal

The MCA checks this signal on boot, and, if asserted low, forces the CC95 SMARC SOM to boot in USB Recovery mode ignoring the SMARC_BOOT_SEL0#, SMARC_BOOT_SEL1# and SMARC_BOOT_SEL2# signals.

VIN_PWR_BAD# signal

The MCA continuously supervises this line. If low, puts the system in poweroff mode, preventing the ConnectCore 95 SMARC module from booting.

MCA firmware update

The i.MX95 processor can update the firmware of the MCA. See the [MCA software documentation](#) for additional information about the MCA firmware update process.

Interfaces

The SMARC specification defines a list of features with different priority levels, which are summarized below:

- **Shall** → indicates a mandatory requirement
- **Should** → Indicates a recommended but not mandatory requirement
- **May** → Indicates a lesser used optional interface
- **Alternate** → Indicates an optional interface, implemented on pins shared with another use

Feature	Sub feature	SMARC requirement	ConnectCore 95 SMARC module implemented	Notes
LVDS LCD	LVDS0 18/24 bit	Should	YES	
	LVDS1 24 bit	May	YES	
DSI on LVDS Pins		May	NO	
HDMI	HDMI display interface	Should	ALTERNATE	Portion of the pins used for MIPI DSI/CSI.
DP on HDMI pins		May	NO	
DP++	DisplayPort++	May	NO	
CSI	CSI0 - 2 lane	May	YES	Shared with MIPI DSI.
	CSI1 - 2/4 lane	Should	YES	
	CSI2	May	NO	
	CSI3	May	NO	
SDIO	SDIO (4 bit, for SD cards)	Should	YES	
SPI	SPI0	Should	YES	
	SPI1/QSPI/eSPI	Should	YES	As eSPI.
Audio	I2S0	Should	YES	As SAI.
	I2S2/HDA	Should	YES	As SAI. No Master Clock available.
I2C	Power Management	Shall	RESERVED	Pads connected, but not available for

Feature	Sub feature	SMARC requirement	ConnectCore 95 SMARC module implemented	Notes
				user.
	General Purpose	Shall	YES	
	Camera	Should	YES	For CSI0 and CSI1.
	LCD Display I/D	Should	YES	
	HDMI	Should	NO	
Serial Ports	SER0 (4 wire)	Shall	YES	Used internally by Bluetooth.
	SER1 (2 wire)	Shall	YES	Default console port.
	SER2 (4 wire)	Should	YES	
	SER3 (2 wire)	Should	YES	
CAN Bus	CAN0	May	YES	
	CAN1	May	YES	
USB	USB0	Shall	YES	As USB 2.0 Host.
	USB1	Should	NO	
	USB2	May	YES	As USB 3.0.
	USB3	May	NO	
	USB4	May	NO	
	USB5	May	NO	
PCIe	PCIE_A	Should	YES	
	PCIE_B	May	YES	
	PCIE_C	May	ALTERNATE	10G Ethernet available.
	PCIE_D	May	NO	
SERDES	Alternative use of PCIE_C/D	May	NO	
SATA	SATA Gen 1	Should	ALTERNATE	Additional SS lines of USB2.
	SATA Gen 2/3	May	NO	
GBE	GBE0	Should	YES	
	GBE1	May	YES	

Feature	Sub feature	SMARC requirement	ConnectCore 95 SMARC module implemented	Notes
Watchdog	WDT Out	Should	YES	
GPIO	GPIO[0:11]	Shall	YES	
	GPIO[0:11] interrupt capability	Shall	NO	See GPIO limitation .
	GPIO[12:13]	Should	YES	
	GPIO[12:13] interrupt capability	Should	NO	See GPIO limitation .
	GPIO Camera support	Shall	YES	
	GPIO5 PWM capability	Should	YES	
	GPIO6 Tachin capability	Should	ALTERNATE	See Note1 below.
Management	Power management features	Shall	YES	
	BATLOW#	Should	ALTERNATE	See Note1 below.
	CARRIER_PWR_ON	Shall	YES	
	CARRIER_STBY#	Should	YES	
	CHARGER_PRSTN#	Should	ALTERNATE	See Note1 below.
	CHARGING#	Should	ALTERNATE	See Note1 below.
	VIN_PWR_BAD#	Shall	YES	
	SLEEP#	Should	YES	
	LID#	Should	ALTERNATE	See Note1 below.
	POWER_BTN#	Should	YES	
	RESET_OUT#	Should	ALTERNATE	See Note1 below.
	RESET_IN#	Should	YES	
	TEST#	Should	ALTERNATE	See Note1 below.
	SMB_ALERT#	Should	ALTERNATE	See Note1 below.

Feature	Sub feature	SMARC requirement	ConnectCore 95 SMARC module implemented	Notes
Boot select		Shall	YES	
Force Recov		Should	YES	
JTAG	JTAG connector on module	May	YES	
RTC		Should	YES	

Note 1 These lines are configured as general purpose IOs. The default SMARC functionality can be implemented by the user.

SDIO

The i.MX95 SoC USDCH2 port is available on the following pads of the SMARC module:

SMARC interface	Signal name	Pin number	IO level
SDIO	SD2_DATA0	P39	3.3/1.8V
	SD2_DATA1	P40	3.3/1.8V
	SD2_DATA2	P41	3.3/1.8V
	SD2_DATA3	P42	3.3/1.8V
	SD2_CMD	P34	3.3/1.8V
	SD2_CLK	P36	3.3/1.8V
	SD2_CD#	P35	3.3/1.8V
	SD2_WP	P33	1.8V
	SD2_RESET#	P37	3.3V

See below the different supported modes of the SDIO port:

- All SD 3.0 protocols are supported at full speeds, including: DS, HS, SDR12, SDR25, SDR50, SDR104 and DDR50.
- For SD, maximum supported SDR frequency is 200MHz (SDR104) and maximum DDR frequency is 50 MHz (DDR50).
- eMMC HS200.
- eMMC High Speed DDR, High Speed SDR and less than or equal to 26 MHz MMC legacy protocols.
- For eMMC, maximum supported SDR frequency is 200 MHz (HS200) and maximum DDR frequency is 200 MHz (HS400).

I2C

I2C2, I2C4, I2C5 and I2C7 i.MX95 buses are available on the ConnectCore 95 SMARC module:

SMARC interface	Signal name	Pin number	IO Level
I2C_GP	I2C2_SDA	S49	1.8V
	I2C2_SCL	S48	1.8V
I2C_CAM0	I2C4_SDA	S7	1.8V
	I2C4_SCL	S5	1.8V
I2C_CAM1	I2C5_SDA	S2	1.8V
	I2C5_SCL	S1	1.8V
I2C_LCD	I2C7_SDA	S140	1.8V
	I2C7_SCL	S139	1.8V

These I2C buses are intended to be used for different purposes, as defined by the SMARC standard:

- I2C2: General purpose I2C.
- I2C4: CSI0 camera I2C.
- I2C5: CSI1 camera I2C.
- I2C7: LCD display I2C.

Note The SMARC specification defines an I2C for power management purposes (pins P121 and P122). Although this bus is physically connected to these pins, it is marked as reserved. Any external connection could interfere with internal functionality.

Note The ConnectCore 95 SMARC module does NOT have internal pull-ups on the I2C lines.

SAI

The ConnectCore 95 SMARC module provides two serial audio interfaces:

SMARC interface	Signal name	Pin number	IO Level
I2S0	SAI3_MCLK	S38	1.8V
	SAI3_TXFS	S39	1.8V
	SAI3_TXD	S40	1.8V
	SAI3_RXD	S41	1.8V
	SAI3_TXC	S42	1.8V

SMARC interface	Signal name	Pin number	IO Level
I2S2	SAI5_TXFS	S50	1.8V
	SAI5_TXD	S51	1.8V
	SAI5_RXD	S52	1.8V
	SAI5_TXC	S53	3.3V

Note The Master Clock line available in pin S38 belongs to SAI3. It cannot be used with SAI5 interface.

SPI

There are two SPI interfaces from the i.MX95 CPU available on the SMARC module:

- SPI0
- XSPI (Flex SPI), working as Quad SPI

SMARC interface	Signal name	Pin number	IO level
SPI0	SPI1_SS1	P31	1.8V
	SPI1_SS0	P43	1.8V
	SPI1_SCK	P44	1.8V
	SPI1_MISO	P45	1.8V
	SPI1_MOSI	P46	1.8V
eSPI	XSPI1_SS0	P54	1.8V
	XSPI1_SS1	P55	1.8V
	XSPI1_SCLK	P56	1.8V
	XSPI1_DATA0	P58	1.8V
	XSPI1_DATA1	P57	1.8V
	XSPI1_DATA2	S56	1.8V
	XSPI1_DATA3	S57	1.8V
	XSPI1_ALERT0#	S43	1.8V
	XSPI1_RESET	S58	1.8V

UART

Following the SMARC definition, the ConnectCore 95 SMARC module provides up to four serial (UART) interfaces, coming directly from the i.MX95 SoC:

- SER0: connected to UART5. This 4-wire UART is internally used by the Bluetooth interface, so it is not available externally in wireless variants of the module.

- SER1: connected to UART1. Default debug port of the Cortex-A55.
- SER2: connected to UART7. 4-wire UART available externally.
- SER3: connected to UART3. 2-wire UART available externally.

SMARC interface	Signal name	Pin number	IO level
SER0	UART5_TX	P129	1.8V
	UART5_RX	P130	1.8V
	UART5_RTS	P131	1.8V
	UART5_CTS	P132	1.8V
SER1	CONSOLE_TX	P134	1.8V
	CONSOLE_RX	P135	1.8V
SER2	UART7_TX	P136	1.8V
	UART7_RX	P137	1.8V
	UART7_RTS	P138	1.8V
	UART7_CTS	P139	1.8V
SER3	UART3_TX	P140	1.8V
	UART3_RX	P141	1.8V

CAN

CAN2 and CAN3 i.MX95 buses are available on the ConnectCore 95 SMARC module:

SMARC interface	Signal name	Pin number	IO Level
CAN0	CAN3_TX	P143	1.8V
	CAN3_RX	P144	1.8V
CAN1	CAN2_TX	P145	1.8V
	CAN2_RX	P146	1.8V

Both CAN ports are in compliance with Flexible Data rate (CAN FD) protocol and the CAN 2.0B specification.

USB

The SMARC specification supports up to six ports. The ConnectCore 95 SMARC module supports only two: USB0 and USB2.

SMARC interface	Signal name	Pin number
USB0	USB0_P	P60
	USB0_N	P61
USB2	USB2_P	P69
	USB2_N	P70
	USB2_TX0_P	S71
	USB2_TX0_N	S72
	USB2_RX0_P	S74
	USB2_RX0_N	S75
SATA	USB2_TX1_P	P48
	USB2_TX1_N	P49
	USB2_RX1_P	P51
	USB2_RX1_N	P52

Note The i.MX95 SoC implements a USB Controller and PHY supporting 3.0 operation including USB Type C capabilities. This means that two sets of USB Superspeed SerDes lanes are used. The SMARC only defines one set of SS data lines, so the extra pairs are connected to pins P48, P49, P51 and P52. These pins are defined as SATA lines on the SMARC specification.

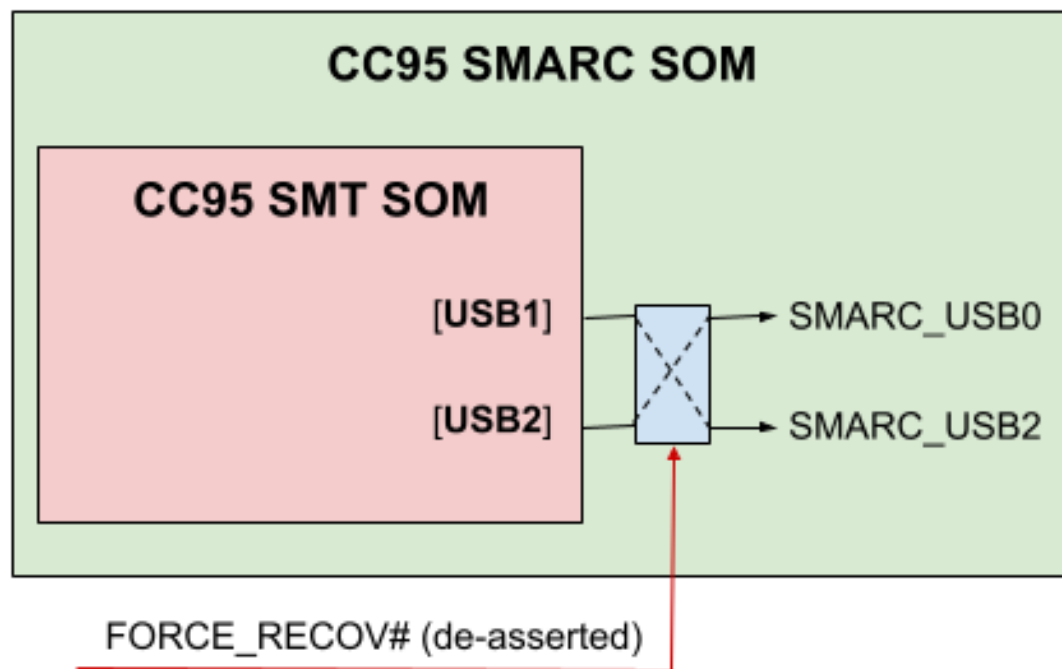
Multiplexing controlled by FORCE_RECOV#

To comply with the SMARC specification requiring specific USB recovery capability, SMARC_USBx ports on the ConnectCore 95 SMARC module are routed differently depending on the status of the FORCE_RECOV# line.

Note NXP documentation uses inconsistent naming for the i.MX95 USB controllers. In this Digi hardware documentation, USB1 refers to the USB 3.0 / SuperSpeed controller, while USB2 refers to the USB 2.0 controller. Note, however, that schematics, NXP datasheet, and pad names refer to the USB 3.0 controller as USB1 (for example, USB1_xx pads), whereas NXP Hardware Reference Manual and Linux device tree sources typically name it USB3. The USB 2.0 controller is consistently associated with USB2 / USB2_xx.

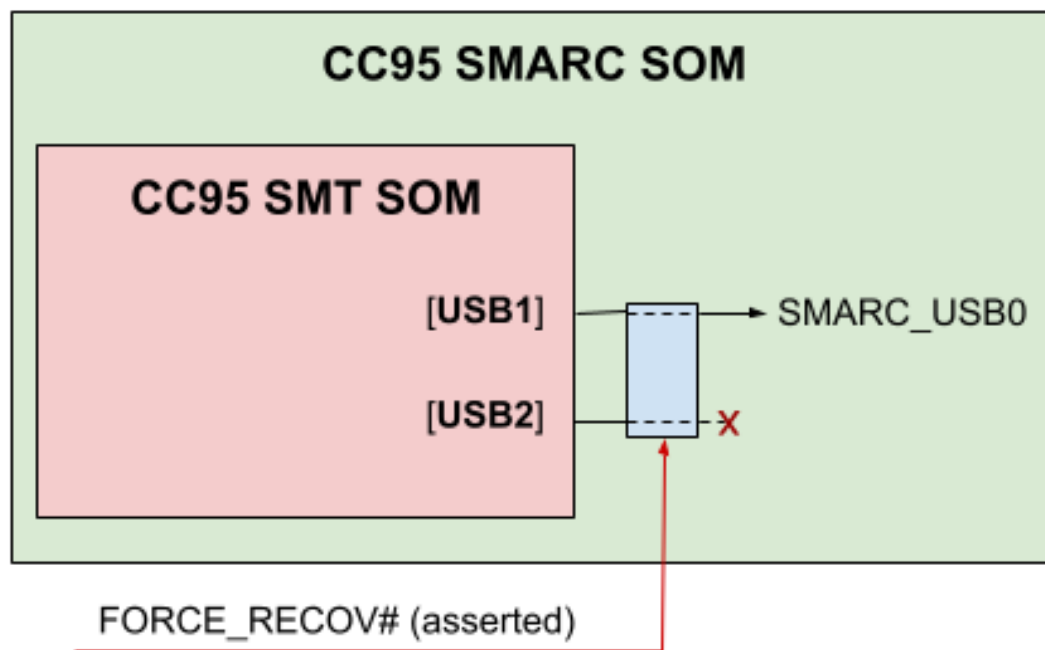
When FORCE_RECOV# is de-asserted:

- CPU USB1 is routed to the SMARC_USB2 port. (According to SMARC specification, this port should support USB 3.2 SuperSpeed.)
- CPU USB2 is routed to the SMARC_USB0 port.



When *FORCE_RECOV#* is asserted:

- CPU USB1 (the only CPU port that can be used for recovery) is routed to SMARC_USB0 port. (According to SMARC specification, this port must be used for recovery.)
- CPU USB2 does not reach the SMARC connector lines; the multiplexer does not route USB2 to the SMARC SOM at all in this case.



Ethernet

The ConnectCore 95 SMARC module supports up to two Gigabit Ethernet interfaces, both of them through Media-dependent interface (MDI) provided by the on-module Ethernet PHYs (LAN8840-VP5A). These PHYs provides RGMII and IEEE 1588v2 support.

SMARC interface	Signal name	Pin number	IO level
GBE0	GBE0_MDI0_N	P29	-
	GBE0_MDI0_P	P30	-
	GBE0_MDI1_N	P26	-
	GBE0_MDI1_P	P27	-
	GBE0_MDI2_N	P23	-
	GBE0_MDI2_P	P24	-
	GBE0_MDI3_N	P19	-
	GBE0_MDI3_P	P20	-
	GBE0_SDP	P6	3.3V
	GBE0_LED1	P25	1.8V
	GBE0_LED4	P22	1.8V
	GBE0_LED5	P21	1.8V
GBE1	GBE1_MDI0_N	S18	-
	GBE1_MDI0_P	S17	-
	GBE1_MDI1_N	S21	-
	GBE1_MDI1_P	S20	-
	GBE1_MDI2_N	S24	-
	GBE1_MDI2_P	S23	-
	GBE1_MDI3_N	S27	-
	GBE1_MDI3_P	S26	-
	GBE1_SDP	P5	3.3V
	GBE1_LED1	S31	1.8V
	GBE1_LED4	S22	1.8V
	GBE1_LED5	S19	1.8V

Together with the MDI lines, the additional SMARC GBE control lines are mapped as follows:

- GBE_x_LED1 → GBE_x_LINK_ACT#
- GBE_x_LED4 → GBE_x_LINK_MAX#
- GBE_x_LED5 → GBE_x_LINK_MID#

Note The GBE_x_LED lines work at 1.8V instead of the specified 3.3V by SMARC.

In addition, the i.MX95 CPU provides one 10G Ethernet interface which is not supported by the SMARC definition. This extra bus is provided on the group of pins dedicated for the PCIE C interface:

SMARC interface	Signal name	Pin number
PCIe C	ETH_TX0_N	S82
	ETH_TX0_P	S81
	ETH_RX0_N	S79
	ETH_RX0_P	S78
	ETH_CLKIN_N	P81
	ETH_CLKIN_P	P80

PCIe

Two PCIe interfaces are supported by the i.MX95 SoC, which are available on the ConnectCore 95 SMARC module.

Note PCIe1 clock differential lines are swapped compared to the SMARC definition:

PCIe1_CLKOUT_N is connected to PCIe_A_REFCK+

PCIe1_CLKOUT_P is connected to PCIe_A_REFCK-

SMARC interface	Signal name	Pin number	IO level
PCIe A	PCIe1_TX0_N	P90	-
	PCIe1_TX0_P	P89	-
	PCIe1_RX0_N	P87	-
	PCIe1_RX0_P	P86	-
	PCIe1_CLKOUT_N	P83	-
	PCIe1_CLKOUT_P	P84	-
	PCIe_A_CKREQ#	P78	3.3V
	PCIe_A_RST#	P75	1.8V
PCIe B	PCIe2_TX0_N	S91	-
	PCIe2_TX0_P	S90	-
	PCIe2_RX0_N	S88	-
	PCIe2_RX0_P	S87	-
	PCIe2_CLKOUT_N	S85	-
	PCIe2_CLKOUT_P	S84	-
	PCIe_B_CKREQ#	P77	3.3V
	PCIe_B_RST#	S76	1.8V

Note PCIE_x_RST# lines work at 1.8V instead of the specified 3.3V by SMARC.

LVDS

The ConnectCore 95 SMARC module supports two LVDS (EIA-644-A standard) channels which can work as follows:

- Single channel output.
- Dual channel output (one input source, two channels outputs for two displays).
- Split channel output (one input source, split to two channels on output).
- Separate 2 channel output.

Both channels support 1080p resolution and can be configured to work as two, 4-lane channels or one single 8-lane channel.

SMARC interface	Signal name	Pin number
LVDS0	LVDS0_D0_N	S126
	LVDS0_D0_P	S125
	LVDS0_D1_N	S129
	LVDS0_D1_P	S128
	LVDS0_D2_N	S132
	LVDS0_D2_P	S131
	LVDS0_D3_N	S138
	LVDS0_D3_P	S137
	LVDS0_CLK_N	S135
	LVDS0_CLK_P	S134
	LCD0_VDD_EN	S133
	LCD0_BKLT_EN	S127
	LCD0_BKLT_PWM	S141

SMARC interface	Signal name	Pin number
LVDS1	LVDS1_D0_N	S112
	LVDS1_D0_P	S111
	LVDS1_D1_N	S115
	LVDS1_D1_P	S114
	LVDS1_D2_N	S118
	LVDS1_D2_P	S117
	LVDS1_D3_N	S121
	LVDS1_D3_P	S120
	LVDS1_CLK_N	S109
	LVDS1_CLK_P	S108
	LCD1_VDD_EN	S116
	LCD1_BKLT_EN	S107
	LCD1_BKLT_PWM	S122

MIPI DSI

The i.MX95 CPU provides one 4-lane MIPI DSI interface through a MIPI-CSI/DSI Combo, which can also work as MIPI CSI. Since the SMARC does not define an interface for MIPI DSI, this interface is connected to the SMARC CSI0 port to keep compatibility when used as a camera interface:

SMARC interface	Signal name	Pin number
CSI0	MIPI_DSI1_DATA0_N	S12
	MIPI_DSI1_DATA0_P	S11
	MIPI_DSI1_DATA1_N	S15
	MIPI_DSI1_DATA1_P	S14
	MIPI_DSI1_CLK_N	S9
	MIPI_DSI1_CLK_P	S8
HDMI	MIPI_DSI1_DATA2_N	P96
	MIPI_DSI1_DATA2_P	P95
	MIPI_DSI1_DATA3_N	P93
	MIPI_DSI1_DATA3_P	P92

Note The two extra data pairs supported by the i.MX95 SoC are connected to HDMI port pins, since this interface is not supported on the ConnectCore 95 SMARC module.

MIPI CSI

The ConnectCore 95 SMARC module supports two, 4-lane MIPI CSI interfaces:

SMARC interface	Signal name	Pin number
CSI0	MIPI_DSI1_DATA0_N	S12
	MIPI_DSI1_DATA0_P	S11
	MIPI_DSI1_DATA1_N	S15
	MIPI_DSI1_DATA1_P	S14
	MIPI_DSI1_CLK_N	S9
	MIPI_DSI1_CLK_P	S8
	GPIO0/CAM0_PWR#	P108
	GPIO2/CAM0_RST#	P110
HDMI	MIPI_DSI1_DATA2_N	P96
	MIPI_DSI1_DATA2_P	P95
	MIPI_DSI1_DATA3_N	P93
	MIPI_DSI1_DATA3_P	P92
CSI1	MIPI_CSI1_DATA0_N	P8
	MIPI_CSI1_DATA0_P	P7
	MIPI_CSI1_DATA1_N	P11
	MIPI_CSI1_DATA1_P	P10
	MIPI_CSI1_DATA2_N	P14
	MIPI_CSI1_DATA2_P	P13
	MIPI_CSI1_DATA3_N	P17
	MIPI_CSI1_DATA3_P	P16
	MIPI_CSI1_CLK_N	P4
	MIPI_CSI1_CLK_P	P3
	GPIO1/CAM1_PWR#	P109
	GPIO3/CAM1_RST#	P111

As explained in [MIPI DSI](#), CSI0 port (which can be configured to work as MIPI DSI) has 4 data lines. The two extra data lines are connected to pins that belong to the SMARC HDMI port.

Signals and multiplexing

Primary (top) side	45
Secondary (bottom) side	54

Primary (top) side

SMARC pin	ConnectCore 95 SMARC module name	i.MX95 / STM uC pin name	Multiplexing (green value represents default functionality)
P1	SMB_ALERT#	GPIO_IO33	ALT0: GPIO5_IO13 ALT2: LPUART6_RX ALT4: LPSPI4_PCS1
P2	GND		
P3	MIPI_CSI1_CLK_P		
P4	MIPI_CSI1_CLK_N		
P5	GBE1_SDP	CCM_CLKO4	ALT0: CLKO_4 ALT1: NETC_TMR_1588_PP2 ALT2: CAN3_RX ALT4: FLEXIO2_FLEXIO29 ALT5: GPIO4_IO29
P6	GBE0_SDP	CCM_CLKO2	ALT0: CLKO_2 ALT1: NETC_TMR_1588_PP1 ALT4: FLEXIO1_FLEXIO27 ALT5: GPIO3_IO27
P7	MIPI_CSI1_DATA0_P		
P8	MIPI_CSI1_DATA0_N		
P9	GND		
P10	MIPI_CSI1_DATA1_P		
P11	MIPI_CSI1_DATA1_N		
P12	GND		
P13	MIPI_CSI1_DATA2_P		
P14	MIPI_CSI1_DATA2_N		
P15	GND		
P16	MIPI_CSI1_DATA3_P		
P17	MIPI_CSI1_DATA3_N		
P18	GND		
P19	GBE0_MDI3_N		
P20	GBE0_MDI3_P		
P21	GBE0_LED5		

SMARC pin	ConnectCore 95 SMARC module name	i.MX95 / STM uC pin name	Multiplexing (green value represents default functionality)
P22	GBE0_LED4		
P23	GBE0_MDI2_N		
P24	GBE0_MDI2_P		
P25	GBE0_LED1		
P26	GBE0_MDI1_N		
P27	GBE0_MDI1_P		
P28	NC		
P29	GBE0_MDIO_N		
P30	GBE0_MDIO_P		
P31	SPI1_SS1	PDM_BIT_STREAM0	ALT0: PDM_BIT_STREAM00 ALT1: MQS1_RIGHT ALT2: LPSP1_PCS1 ALT3: TPM1_EXTCLK ALT4: LPTMR1_ALT2 ALT5: GPIO1_IO09 ALT6: CAN1_RX
P32	GND		
P33	SDIO_WP	PB9	
P34	SD2_CMD	SD2_CMD	ALT0: USDHC2_CMD ALT1: NETC_TMR_1588_TRIG2 ALT2: I3C2_PUR ALT3: I3C2_PUR_B ALT4: FLEXIO1_FLEXIO02 ALT5: GPIO3_IO02
P35	SD2_CD#	SD2_CD_B	ALT0: USDHC2_CD_B ALT1: NETC_TMR_1588_TRIG1 ALT2: I3C2_SCL ALT4: FLEXIO1_FLEXIO00 ALT5: GPIO3_IO00
P36	SD2_CLK	SD2_CLK	ALT0: USDHC2_CLK ALT1: NETC_TMR_1588_PP1 ALT2: I3C2_SDA ALT4: FLEXIO1_FLEXIO01 ALT5: GPIO3_IO01
P37	SD2_RESET#	SD2_RESET_B	ALT0: USDHC2_RESET_B ALT1: LPTMR2_ALT2 ALT3: NETC_TMR_1588_GCLK ALT4: FLEXIO1_FLEXIO07 ALT5: GPIO3_IO07

SMARC pin	ConnectCore 95 SMARC module name	i.MX95 / STM uC pin name	Multiplexing (green value represents default functionality)
P38	GND		
P39	SD2_DATA0	SD2_DATA0	ALT0: USDHC2_DATA0 ALT1: NETC_TMR_1588_PP2 ALT2: CAN2_TX ALT4: FLEXIO1_FLEXIO03 ALT5: GPIO3_IO03
P40	SD2_DATA1	SD2_DATA1	ALT0: USDHC2_DATA1 ALT1: NETC_TMR_1588_CLK ALT2: CAN2_RX ALT4: FLEXIO1_FLEXIO04 ALT5: GPIO3_IO04
P41	SD2_DATA2	SD2_DATA2	ALT0: USDHC2_DATA2 ALT1: NETC_TMR_1588_PP3 ALT2: MQS2_RIGHT ALT4: FLEXIO1_FLEXIO05 ALT5: GPIO3_IO05
P42	SD2_DATA3	SD2_DATA3	ALT0: USDHC2_DATA3 ALT1: LPTMR2_ALT1 ALT2: MQS2_LEFT ALT3: NETC_TMR_1588_ALARM1 ALT4: FLEXIO1_FLEXIO06 ALT5: GPIO3_IO06
P43	SPI1_SS0	SAI1_TXFS	ALT0: SAI1_TX_SYNC ALT1: SAI1_TX_DATA01 ALT2: LPSPI1_PCS0 ALT3: LPUART2_DTR_B ALT4: MQS1_LEFT ALT5: GPIO1_IO11
P44	SPI1_SCK	SAI1_TXD0	ALT0: SAI1_TX_DATA00 ALT1: LPUART2_RTS_B ALT2: LPSPI1_SCK ALT3: LPUART1_DTR_B ALT4: CAN1_TX ALT5: GPIO1_IO13
P45	SPI1_MISO	SAI1_TXC	ALT0: SAI1_TX_BCLK ALT1: LPUART2_CTS_B ALT2: LPSPI1_SIN ALT3: LPUART1_DSR_B ALT4: CAN1_RX ALT5: GPIO1_IO12
P46	SPI1_MOSI	SAI1_RXD0	ALT0: SAI1_RX_DATA00 ALT1: SAI1_MCLK ALT2: LPSPI1_SOUT ALT3: LPUART2_DSR_B

SMARC pin	ConnectCore 95 SMARC module name	i.MX95 / STM uC pin name	Multiplexing (green value represents default functionality)
			ALT4: MQS1_RIGHT ALT5: GPIO1_IO14
P47	GND		
P48	USB2_TX1_P	USB1_TX1_P	
P49	USB2_TX1_N	USB1_TX1_N	
P50	GND		
P51	USB2_RX1_P	USB1_RX1_N	
P52	USB2_RX1_N	USB1_RX1_N	
P53	GND		
P54	XSPI1_SS0	XSPI1_SS0_B	ALT0: FLEXSPI1_A_SS0_B ALT1: SAI2_RX_DATA05 ALT2: SAI4_RX_BCLK ALT3: EARC_CEC_OUT ALT4: XSPI_CS ALT5: GPIO5_IO10
P55	XSPI1_SS1	XSPI1_SS1_B	ALT0: FLEXSPI1_A_SS1_B ALT1: SAI5_RX_BCLK ALT2: SAI5_TX_DATA03 ALT3: SAI2_RX_DATA07 ALT5: GPIO5_IO11
P56	XSPI1_SCLK	XSPI1_SCLK	ALT0: FLEXSPI1_A_SCLK ALT1: SAI2_RX_DATA04 ALT2: SAI4_RX_SYNC ALT3: EARC_DC_HPD_IN ALT4: XSPI_CLK ALT5: GPIO5_IO09
P57	XSPI1_DATA1	XSPI1_DATA1	ALT0: FLEXSPI1_A_DATA01 ALT1: SAI2_TX_DATA05 ALT2: SAI4_TX_SYNC ALT3: SAI4_TX_DATA01 ALT4: XSPI_DATA01 ALT5: GPIO5_IO01
P58	XSPI1_DATA0	XSPI1_DATA0	ALT0: FLEXSPI1_A_DATA00 ALT1: SAI2_TX_DATA04 ALT2: SAI4_TX_BCLK ALT3: SAI4_RX_DATA01 ALT4: XSPI_DATA00 ALT5: GPIO5_IO00
P59	GND		
P60	USB0_P		

SMARC pin	ConnectCore 95 SMARC module name	i.MX95 / STM uC pin name	Multiplexing (green value represents default functionality)
P61	USB0_N		
P62	USB0_EN_OC#		
P63	USB0_VBUS_DET		
P64	USB0_ID		
P65	USB1_P		
P66	USB1_N		
P67	USB1_EN_OC#		
P68	GND		
P69	USB2_P		
P70	USB2_N		
P71	USB2_EN_OC#	ENET1_MDIO	ALT0: NETC_MDIO ALT1: LPUART3_RIN_B ALT2: I3C2_SDA ALT3: USB1_OTG_PWR ALT4: FLEXIO2_FLEXIO01 ALT5: GPIO4_IO01
P72	RESERVED		
P73	NC		
P74	USB3_EN_OC#		
P75	PCIE_A_RST#	PB10	
P76	USB4_EN_OC#		
P77	PCIE_B_CKREQ#	GPIO_IO35	ALT0: GPIO5_IO15 ALT1: PCIE2_CLKREQ_B ALT2: LPUART6_RTS_B ALT4: LPSP14_SIN
P78	PCIE_A_CKREQ#	GPIO_IO32	ALT0: GPIO5_IO12 ALT1: PCIE1_CLKREQ_B ALT2: LPUART6_TX ALT4: LPSP14_PCS2
P79	GND		
P80	ETH_CLKIN_P		
P81	ETH_CLKIN_N		
P82	GND		
P83	PCIE1_CLKOUT_P		

SMARC pin	ConnectCore 95 SMARC module name	i.MX95 / STM uC pin name	Multiplexing (green value represents default functionality)
P84	PCIE1_CLKOUT_N		
P85	GND		
P86	PCIE1_RX0_P		
P87	PCIE1_RX0_N		
P88	GND		
P89	PCIE1_TX0_P		
P90	PCIE1_TX0_N		
P91	GND		
P92	MIPI_DSI1_DATA3_P		
P93	MIPI_DSI1_DATA3_N		
P94	GND		
P95	MIPI_DSI1_DATA2_P		
P96	MIPI_DSI1_DATA2_N		
P97	GND		
P98	NC		
P99	NC		
P100	GND		
P101	NC		
P102	NC		
P103	GND		
P104	NC		
P105	NC		
P106	NC		
P107	NC		
P108	GPIO0/CAM0_PWR#	PB15	
P109	GPIO1/CAM1_PWR#	PB14	
P110	GPIO2/CAM0_RST#	PB13	
P111	GPIO3/CAM1_RST#	PB12	
P112	GPIO4/HDA_RST#	PB11	
P113	GPIO5/PWM_OUT	GPIO_IO24	ALTO: GPIO2_IO24

SMARC pin	ConnectCore 95 SMARC module name	i.MX95 / STM uC pin name	Multiplexing (green value represents default functionality)
			ALT1: USDHC3_DATA0 ALT4: TPM3_CH3 ALT5: JTAG_MUX_TDO ALT6: LPSPI6_PCS1 ALT7: FLEXIO1_FLEXIO24
P114	GPIO6/TACHIN	UART2_RXD	ALT0: LPUART2_RX ALT1: LPUART1_CTS_B ALT2: LPSPI2_SOUT ALT3: TPM1_CH2 ALT4: SAI1_MCLK ALT5: GPIO1_IO06
P115	GPIO7	PA14	
P116	GPIO8	ENET1_MDC	ALT0: NETC_MDC ALT1: LPUART3_DCD_B ALT2: I3C2_SCL ALT3: USB1_OTG_ID ALT4: FLEXIO2_FLEXIO00 ALT5: GPIO4_IO00
P117	GPIO9	PA11	
P118	GPIO10	PDM_CLK	ALT0: PDM_CLK ALT1: MQS1_LEFT ALT4: LPTMR1_ALT1 ALT5: GPIO1_IO08 ALT6: CAN1_TX
P119	GPIO11	PA15	
P120	GND		
P121	NC		
P122	NC		
P123	BOOT_SEL0#		
P124	BOOT_SEL1#		
P125	BOOT_SEL2#		
P126	RESET_OUT#		
P127	RESET_IN#		
P128	PWR_BTN#		
P129	UART7_TX	GPIO_IO36	ALT0: GPIO5_IO16 ALT2: LPUART7_TX ALT4: LPSPI4_SOUT
P130	UART7_RX	GPIO_IO37	ALT0: GPIO5_IO17

SMARC pin	ConnectCore 95 SMARC module name	i.MX95 / STM uC pin name	Multiplexing (green value represents default functionality)
			ALT2: LPUART7_RX ALT4: LPSP14_SCK
P131	UART7_RTS	GPIO_IO11	ALT0: GPIO2_IO11 ALT1: LPSP13_SCK ALT4: TPM5_EXTCLK ALT5: LPUART7_RTS_B ALT6: LPI2C8_SCL ALT7: FLEXIO1_FLEXIO11
P132	UART7_CTS	GPIO_IO10	ALT0: GPIO2_IO10 ALT1: LPSP13_SOUT ALT4: TPM4_EXTCLK ALT5: LPUART7_CTS_B ALT6: LPI2C8_SDA ALT7: FLEXIO1_FLEXIO10
P133	GND		
P134	CONSOLE_TX	UART1_TXD	ALT0: LPUART1_TX ALT1: ELE_UART_TX ALT2: LPSP12_PCS0 ALT3: TPM1_CH1 ALT5: GPIO1_IO05
P135	CONSOLE_RX	UART1_RXD	ALT0: LPUART1_RX ALT1: ELE_UART_RX ALT2: LPSP12_SIN ALT3: TPM1_CH0 ALT5: GPIO1_IO04
P136	UART5_TX	GPIO_IO00	ALT0: GPIO2_IO00 ALT1: LPI2C3_SDA ALT4: LPSP16_PCS0 ALT5: LPUART5_TX ALT6: LPI2C5_SDA ALT7: FLEXIO1_FLEXIO00
P137	UART5_RX	GPIO_IO01	ALT0: GPIO2_IO01 ALT1: LPI2C3_SCL ALT4: LPSP16_SIN ALT5: LPUART5_RX ALT6: LPI2C5_SCL ALT7: FLEXIO1_FLEXIO01
P138	UART5_RTS	GPIO_IO03	ALT0: GPIO2_IO03 ALT1: LPI2C4_SCL ALT4: LPSP16_SCK ALT5: LPUART5_RTS_B ALT6: LPI2C6_SCL ALT7: FLEXIO1_FLEXIO03
P139	UART5_CTS	GPIO_IO02	ALT0: GPIO2_IO02

SMARC pin	ConnectCore 95 SMARC module name	i.MX95 / STM uC pin name	Multiplexing (green value represents default functionality)
			ALT1: LPI2C4_SDA ALT4: LPSP16_SOUT ALT5: LPUART5_CTS_B ALT6: LPI2C6_SDA ALT7: FLEXIO1_FLEXIO02
P140	UART3_TX	GPIO_IO14	ALT0: GPIO2_IO14 ALT1: LPUART3_TX ALT4: LPSP18_SOUT ALT5: LPUART8_CTS_B ALT6: LPUART4_TX ALT7: FLEXIO1_FLEXIO14
P141	UART3_RX	GPIO_IO15	ALT0: GPIO2_IO15 ALT1: LPUART3_RX ALT4: LPSP18_SCK ALT5: LPUART8_RTS_B ALT6: LPUART4_RX ALT7: FLEXIO1_FLEXIO15
P142	GND		
P143	CAN3_TX	GPIO_IO28	ALT0: GPIO2_IO28 ALT1: LPI2C3_SDA ALT2: CAN3_TX ALT7: FLEXIO1_FLEXIO28
P144	CAN3_RX	GPIO_IO29	ALT0: GPIO2_IO29 ALT1: LPI2C3_SCL ALT2: CAN3_RX ALT3: FLEXIO1_FLEXIO29
P145	CAN2_TX	GPIO_IO25	ALT0: GPIO2_IO25 ALT1: USDHC3_DATA1 ALT2: CAN2_TX ALT4: TPM4_CH3 ALT5: JTAG_MUX_TCK ALT6: LPSP17_PCS1 ALT7: FLEXIO1_FLEXIO25
P146	CAN2_RX	GPIO_IO27	ALT0: GPIO2_IO27 ALT1: USDHC3_DATA3 ALT2: CAN2_RX ALT4: TPM6_CH3 ALT5: JTAG_MUX_TMS ALT6: LPSP15_PCS1 ALT7: FLEXIO1_FLEXIO27
P147	VDD_IN		
P148	VDD_IN		
P149	VDD_IN		

SMARC pin	ConnectCore 95 SMARC module name	i.MX95 / STM uC pin name	Multiplexing (green value represents default functionality)
P150	VDD_IN		
P151	VDD_IN		
P152	VDD_IN		
P153	VDD_IN		
P154	VDD_IN		
P155	VDD_IN		
P156	VDD_IN		

Secondary (bottom) side

SMARC pin	ConnectCore 95 SMARC module name	i.MX95 / STM uC pin name	Multiplexing (green value represents default functionality)
S1	I2C5_SCL	GPIO_IO23	ALT0: GPIO2_IO23 ALT1: USDHC3_CMD ALT2: SPDIF_OUT ALT3: CAN5_RX ALT4: TPM6_CH1 ALT6: LPI2C5_SCL ALT7: FLEXIO1_FLEXIO23
S2	I2C5_SDA	GPIO_IO22	ALT0: GPIO2_IO22 ALT1: USDHC3_CLK ALT2: SPDIF_IN ALT3: CAN5_TX ALT4: TPM5_CH1 ALT5: TPM6_EXTCLK ALT6: LPI2C5_SDA ALT7: FLEXIO1_FLEXIO22
S3	GND		
S4	NC		
S5	I2C4_SCL	GPIO_IO31	ALT0: GPIO2_IO31 ALT1: LPI2C4_SCL ALT2: CAN5_RX ALT7: FLEXIO1_FLEXIO31
S6	CCM_CLKO1/IO3_26	CCM_CLKO1	ALT0: CLKO_1 ALT1: NETC_TMR_1588_TRIG1 ALT4: FLEXIO1_FLEXIO26 ALT5: GPIO3_IO26
S7	I2C4_SDA	GPIO_IO30	ALT0: GPIO2_IO30

SMARC pin	ConnectCore 95 SMARC name	i.MX95 / STM uC pin name	Multiplexing (green value represents default functionality)
			ALT1: LPI2C4_SDA ALT2: CAN5_TX ALT7: FLEXIO1_FLEXIO30
S8	MIPI_DSI1_CLK_P		
S9	MIPI_DSI1_CLK_N		
S10	GND		
S11	MIPI_DSI1_DATA0_P		
S12	MIPI_DSI1_DATA0_N		
S13	GND		
S14	MIPI_DSI1_DATA1_P		
S15	MIPI_DSI1_DATA1_N		
S16	GND		
S17	GBE1_MDIO_P		
S18	GBE1_MDIO_N		
S19	GBE1_LED5		
S20	GBE1_MDIO1_P		
S21	GBE1_MDIO1_N		
S22	GBE1_LED4		
S23	GBE1_MDIO2_P		
S24	GBE1_MDIO2_N		
S25	GND		
S26	GBE1_MDIO3_P		
S27	GBE1_MDIO3_N		
S28	NC		
S29	NC		
S30	NC		
S31	GBE1_LED1		
S32	NC		
S33	NC		
S34	GND		

SMARC pin	ConnectCore 95 SMARC name	i.MX95 / STM uC pin name	Multiplexing (green value represents default functionality)
S35	USB4_P		
S36	USB4_N		
S37	NC		
S38	SAI3_MCLK	GPIO_IO17	ALT0: GPIO2_IO17 ALT1: SAI3_MCLK ALT4: LPUART3_RTS_B ALT5: LPSPI4_PCS1 ALT6: LPUART4_RTS_B ALT7: FLEXIO1_FLEXIO17
S39	SAI3_TXFS	GPIO_IO26	ALT0: GPIO2_IO26 ALT1: USDHC3_DATA2 ALT2: PDM_BIT_STREAM01 ALT3: FLEXIO1_FLEXIO26 ALT4: TPM5_CH3 ALT5: JTAG_MUX_TDI ALT6: LPSPI8_PCS1 ALT7: SAI3_TX_SYNC
S40	SAI3_TXD	GPIO_IO21	ALT0: GPIO2_IO21 ALT1: SAI3_TX_DATA00 ALT2: PDM_CLK ALT3: FLEXIO1_FLEXIO21 ALT4: LPSPI5_SCK ALT5: LPSPI4_SCK ALT6: TPM4_CH1 ALT7: SAI3_RX_BCLK
S41	SAI3_RXD	GPIO_IO20	ALT0: GPIO2_IO20 ALT1: SAI3_RX_DATA00 ALT2: PDM_BIT_STREAM00 ALT4: LPSPI5_SOUT ALT5: LPSPI4_SOUT ALT6: TPM3_CH1 ALT7: FLEXIO1_FLEXIO20
S42	SAI3_TXC	GPIO_IO16	ALT0: GPIO2_IO16 ALT1: SAI3_TX_BCLK ALT2: PDM_BIT_STREAM02 ALT4: LPUART3_CTS_B ALT5: LPSPI4_PCS2 ALT6: LPUART4_CTS_B ALT7: FLEXIO1_FLEXIO16
S43	SPI1_ALERT0#	XSPI1_DQS	ALT0: FLEXSPI1_A_DQS ALT1: SAI5_RX_SYNC ALT2: SAI5_TX_DATA02 ALT3: SAI2_RX_DATA06 ALT4: XSPI_DQS ALT5: GPIO5_IO08

SMARC pin	ConnectCore 95 SMARC name	i.MX95 / STM uC pin name	Multiplexing (green value represents default functionality)
S44	NC		
S45	ENET1_MDC	ENET2_MDC	ALT0: NETC_MDC ALT1: LPUART4_DCD_B ALT2: SAI2_RX_SYNC ALT4: FLEXIO2_FLEXIO14 ALT5: GPIO4_IO14
S46	ENET1_MDIO	ENET2_MDIO	ALT0: NETC_MDIO ALT1: LPUART4_RIN_B ALT2: SAI2_RX_BCLK ALT4: FLEXIO2_FLEXIO15 ALT5: GPIO4_IO15
S47	GND		
S48	I2C2_SCL	I2C2_SCL	ALT0: LPI2C2_SCL ALT1: I3C1_PUR ALT2: LPUART2_DCD_B ALT3: TPM2_CH2 ALT4: SAI1_RX_SYNC ALT5: GPIO1_IO02 ALT6: I3C1_PUR_B
S49	I2C2_SDA	I2C2_SDA	ALT0: LPI2C2_SDA ALT2: LPUART2_RIN_B ALT3: TPM2_CH3 ALT4: SAI1_RX_BCLK ALT5: GPIO1_IO03
S50	SAI5_TXFS	XSPI1_DATA5	ALT0: FLEXSPI1_A_DATA05 ALT1: SAI5_TX_SYNC ALT2: SAI5_RX_DATA02 ALT3: SAI2_RX_DATA06 ALT4: XSPI_DATA05 ALT5: GPIO5_IO05
S51	SAI5_TXD	XSPI1_DATA4	ALT0: FLEXSPI1_A_DATA04 ALT1: SAI5_TX_DATA00 ALT2: SAI5_RX_DATA01 ALT4: XSPI_DATA04 ALT5: GPIO5_IO04
S52	SAI5_RXD	XSPI1_DATA7	ALT0: FLEXSPI1_A_DATA07 ALT1: SAI5_RX_DATA00 ALT2: SAI5_TX_DATA01 ALT4: XSPI_DATA07 ALT5: GPIO5_IO07
S53	SAI5_TXC	XSPI1_DATA6	ALT0: FLEXSPI1_A_DATA06 ALT1: SAI5_TX_BCLK ALT2: SAI5_RX_DATA03 ALT3: SAI2_RX_DATA07

SMARC pin	ConnectCore 95 SMARC name	i.MX95 / STM uC pin name	Multiplexing (green value represents default functionality)
			ALT4: XSPI_DATA06 ALT5: GPIO5_IO06
S54	NC		
S55	NC		
S56	XSPI1_DATA2	XSPI1_DATA2	ALT0: FLEXSPI1_A_DATA02 ALT1: SAI2_TX_DATA06 ALT2: SAI4_TX_DATA00 ALT4: XSPI_DATA02 ALT5: GPIO5_IO02
S57	XSPI1_DATA3	XSPI1_DATA3	ALT0: FLEXSPI1_A_DATA03 ALT1: SAI2_TX_DATA07 ALT2: SAI4_RX_DATA00 ALT4: XSPI_DATA03 ALT5: GPIO5_IO03
S58	XSPI1_RESET#	PA12	
S59	NC		
S60	NC		
S61	GND		
S62	NC		
S63	NC		
S64	GND		
S65	NC		
S66	NC		
S67	GND		
S68	USB3_P		
S69	USB3_N		
S70	GND		
S71	USB2_TX0_P		
S72	USB2_TX0_N		
S73	GND		
S74	USB2_RX0_P		
S75	USB2_RX0_N		
S76	PCIE_B_RST#	PB1	

SMARC pin	ConnectCore 95 SMARC name	i.MX95 / STM uC pin name	Multiplexing (green value represents default functionality)
S77	NC		
S78	ETH_RX0_P		
S79	ETH_RX0_N		
S80	GND		
S81	ETH_TX0_P		
S82	ETH_TX0_N		
S83	GND		
S84	PCIE2_CLKOUT_P		
S85	PCIE2_CLKOUT_N		
S86	GND		
S87	PCIE2_RX0_P		
S88	PCIE2_RX0_N		
S89	GND		
S90	PCIE2_TX0_P		
S91	PCIE2_TX0_N		
S92	GND		
S93	NC		
S94	NC		
S95	NC		
S96	NC		
S97	NC		
S98	NC		
S99	NC		
S100	NC		
S101	GND		
S102	NC		
S103	NC		
S104	NC		
S105	NC		

SMARC pin	ConnectCore 95 SMARC name	i.MX95 / STM uC pin name	Multiplexing (green value represents default functionality)
S106	NC		
S107	LCD1_BKLT_EN	PB2	
S108	LVDS1_CLK_P		
S109	LVDS1_CLK_N		
S110	GND		
S111	LVDS1_D0_P		
S112	LVDS1_D0_N		
S113	NC		
S114	LVDS1_D1_P		
S115	LVDS1_D1_N		
S116	LCD1_VDD_EN	PB3	
S117	LVDS1_D2_P		
S118	LVDS1_D2_N		
S119	GND		
S120	LVDS1_D3_P		
S121	LVDS1_D3_N		
S122	LCD1_BKLT_PWM	GPIO_IO04	ALT0: GPIO2_IO04 ALT1: TPM3_CH0 ALT2: PDM_CLK ALT3: CAN4_TX ALT4: LPSPI7_PCS0 ALT5: LPUART6_TX ALT6: LPI2C6_SDA ALT7: FLEXIO1_FLEXIO04
S123	GPIO13	PF3	
S124	GND		
S125	LVDS0_D0_P		
S126	LVDS0_D0_N		
S127	LCD0_BKLT_EN	PB4	
S128	LVDS0_D1_P		
S129	LVDS0_D1_N		
S130	GND		

SMARC pin	ConnectCore 95 SMARC name	i.MX95 / STM uC pin name	Multiplexing (green value represents default functionality)
S131	LVDS0_D2_P		
S132	LVDS0_D2_N		
S133	LCD0_VDD_EN	PB5	
S134	LVDS0_CLK_P		
S135	LVDS0_CLK_N		
S136	GND		
S137	LVDS_D3_P		
S138	LVDS_D3_N		
S139	I2C7_SCL	GPIO_IO09	ALT0: GPIO2_IO09 ALT1: LPSPI3_SIN ALT4: TPM3_EXTCLK ALT5: LPUART7_RX ALT6: LPI2C7_SCL ALT7: FLEXIO1_FLEXIO09
S140	I2C7_SDA	GPIO_IO08	ALT0: GPIO2_IO08 ALT1: LPSPI3_PCS0 ALT4: TPM6_CH0 ALT5: LPUART7_TX ALT6: LPI2C7_SDA ALT7: FLEXIO1_FLEXIO08
S141	LCD0_BKLT_PWM	GPIO_IO05	ALT0: GPIO2_IO05 ALT1: TPM4_CH0 ALT2: PDM_BIT_STREAM00 ALT3: CAN4_RX ALT4: LPSPI7_SIN ALT5: LPUART6_RX ALT6: LPI2C6_SCL ALT7: FLEXIO1_FLEXIO05
S142	GPIO12	PF1	
S143	GND		
S144	NC		
S145	WDT_TIME_OUT#		
S146	PCIE_WAKE#	PB8	
S147	VDD_RTC		
S148	LID#	PC13	
S149	SLEEP#		

SMARC pin	ConnectCore 95 SMARC name	i.MX95 / STM uC pin name	Multiplexing (green value represents default functionality)
S150	VIN_PWR_BAD#		
S151	CHARGING#	PA4	
S152	CHARGER_PRSENT#	PA5	
S153	CARRIER_STBY#		
S154	CARRIER_PWR_ON		
S155	FORCE_RECOV#		
S156	BATLOW#	PA9	
S157	TEST#	PA10	
S158	GND		

Module specifications

The following sections describe the specifications for the ConnectCore 95 SMARC module.

Electrical specification 64

Environmental specifications 64

Electrical specification

The ConnectCore 95 SMARC module has two supply inputs. One is the primary input power supply to the whole module, while the other one powers the RTC of the module when the main supply is not present. The following table shows the voltage range of these input supplies:

Signal	Description	Min	Typ	Max	Unit
VDD_IN	Main power supply to module	3.7	5	5.5	V
VDD_RTC	RTC backup power supply	1.55	-	3.6	V

Environmental specifications

Operating temperature: -40 to 85 °C.



CAUTION! Your final product may require additional thermal management such as passive (heatsink/spreader) or active (airflow) cooling to achieve the maximum operating temperature without exceeding the processor junction temp limit.
