ConnectCore 91

System-on-Module

Hardware Reference Manual

Revision history—90002600

Revision	Date	Description
1P	October 2024	Initial release.
2P	June 2025	Fixed number of CAN interfaces; removed LCDIF; added parallel display note; marked LVDS pads as "NC"; added new section linking to ConnectCore 9 series compatibility guide; added Socket options topic; added block diagram.
3P	April 2026	Added Assembly instructions.
4P	August 2026	Modified and expanded entries for pads Y1, AH6, and AH12 and castellated pad 95; replaced transmit power and data rate tables and removed note; added MTBF section; added SOM weight and link to support resources; misc minor fixes.

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About the ConnectCore 91 SOM

Features and functionality

The ConnectCore 91 system-on-module is based on the i.MX 91 processor from NXP. This processor offers a number of interfaces, most of them multiplexed and not available simultaneously. The module has the following features:

- Single Cortex-A55 processor:
  - Frequency operating at up to 1.4 GHz.
  - 32 KB L1 instruction cache.
  - 32 KB L1 data cache.
  - 256 KB L2 cache.
  - Media Processing Engine (MPE) with ARM NEON technology supporting the Advanced Single Instruction Multiple Data architecture.
  - Floating Point Unit (FPU) with support of the Arm VFPv4-D16 architecture.
  - Support of 64-bit Arm v8.2-A architecture.
  - Parity/ECC protection on L1 cache, L2 cache, and TLB RAMs.
  - Boot ROM (256 KB).
  - On-chip RAM (384 KB).
  - Security:
    - Trusted resource domain controller (TRDC).
    - ARM TrustZone (TZ) architecture, including Trustzone-A.
    - On-chip RAM (OCRAM) secure region protection using OCRAM controller.
    - EdgeLock secure enclave.
    - Battery backed security module (BBSM):
      - Secure non-volatile storage (SNVS).
      - Secure real-time clock (RTC).
- System debug:
  - Arm CoreSight debug and trace technology.
  - Embedded trace FIFO (ETF) with 4 KB internal storage to provide trace buffering.
  - Unified trace capability for single core Cortex-A55.
  - Cross Triggering Interface (CTI).
  - 4-pin JTAG.
- Image sensor interface (ISI):
  - Standard pixel formats commonly used in many camera input protocols.
  - Programmable resolutions up to 2K.

    - Image processing for:
        - Supports one source of up to 2K horizontal resolution.
        - Supports pixel rate up to 200 Mpixel/s.
    - Image down scaling via decimation and bi-phase filtering.
    - Color space conversion.
    - Interlaced to progressive conversions.
- Connectivity:
    - x2 USB 2.0 controllers and PHYs interfaces.
    - x2 CAN/CAN-FD.
    - x2 I3C.
    - x2 32-pin FlexIO modules.
    - x3 uSDHC.
    - x2 Ethernet controllers:
        - x1 Gigabit Ethernet controller with support for Energy Efficient Ethernet (EEE), Ethernet AVB and IEEE 1588.
        - x1 Gigabit Ethernet controller with support for TSN in addition to EEE, Ethernet AVB and IEEE 1588.
    - x8 LPSPI.
    - x8 I2C.
    - x8 LPUART.
- Multimedia:
    - Parallel camera
    - Audio:
        - x3 SAI interfaces:
            - SAI1 supports 2 lanes TX and 1 lane RX
            - SAI2 supports 1 lane TX and 1 lane RX
            - SAI3 supports 1 lane TX and 1 lane RX
            - x1 SPDIF
            - 24-bit PDM supports up to 8-microphones (4 lanes)
- Up to 512 MB, 16-bit LPDDR4 memory.
- Up to 8 GB, 8-bit eMMC memory.
- NXP PCA9451 Power Management IC (PMIC):
    - x6 Step down regulators.
    - x5 Linear regulators.
    - x1 Load switch.
- IEEE 802.11 a/b/g/n/ac/ax WLAN interface.
- Bluetooth version 5.4.

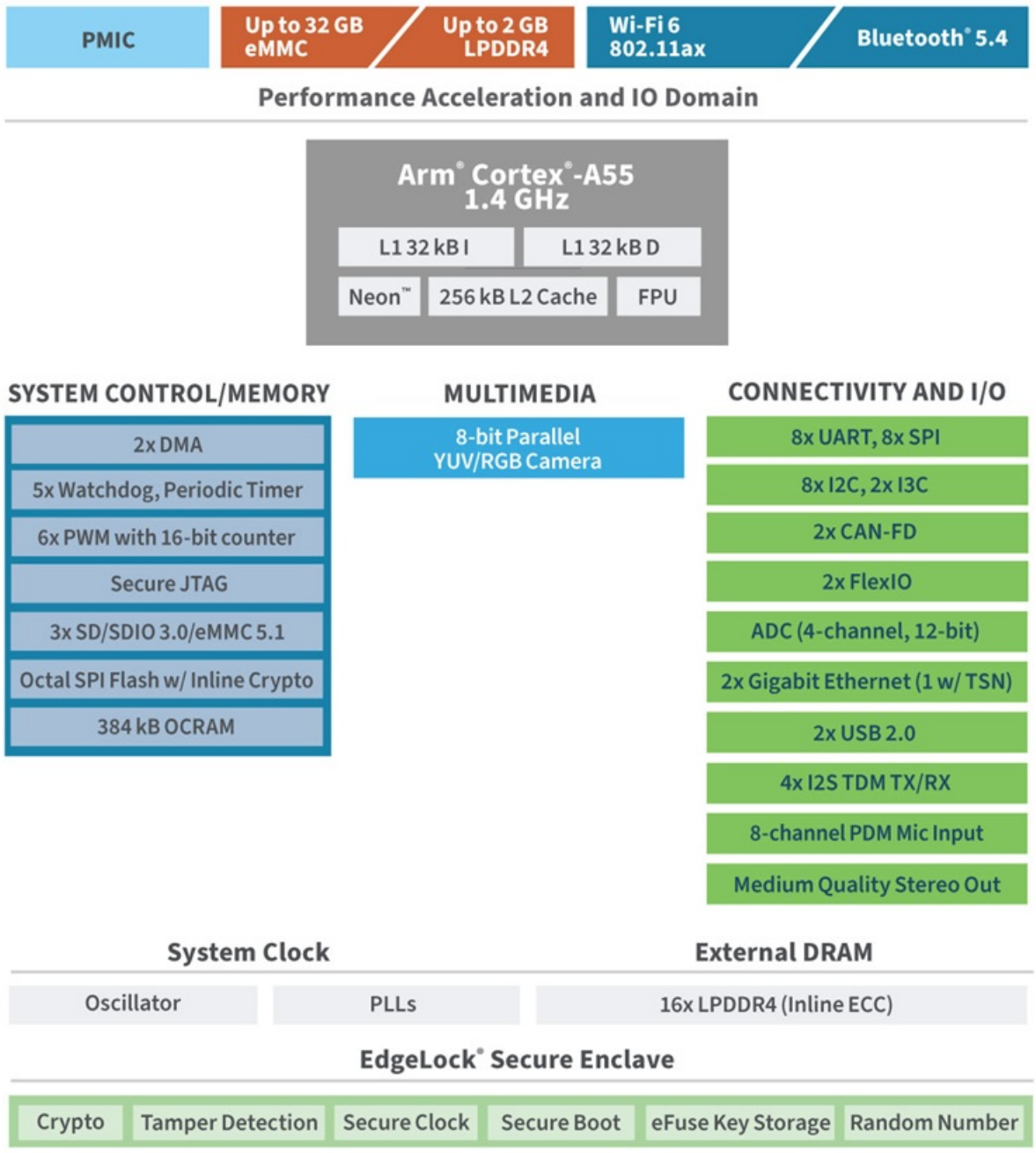
Safety instructions

- The ConnectCore 91 SOM cannot be guaranteed operation due to the radio link and so should not be used for interlocks in safety critical devices such as machines or automotive applications.
- The ConnectCore 91 SOM has not been approved for use in (this list is not exhaustive):
  - nuclear applications
  - explosive or flammable atmospheres
- There are no user serviceable components inside the ConnectCore 91 SOM. Do not modify the ConnectCore 91 in any way. Modifications may exclude the SOM from any warranty and can cause the ConnectCore 91 to operate outside of regulatory compliance for a given country, leading to the possible illegal operation of the radio.
- Use industry standard ESD protection when handling the ConnectCore 91 SOM.
- Take care while handling to avoid electrical damage to the PCB and components.
- Do not expose ConnectCore 91 SOM to water or moisture.
- Use this product with the antennas specified in the ConnectCore 91 SOM user guides.
- The end user must be told how to remove power from the ConnectCore 91 SOM or to locate the antennas 20 cm from humans or animals.

Block diagrams

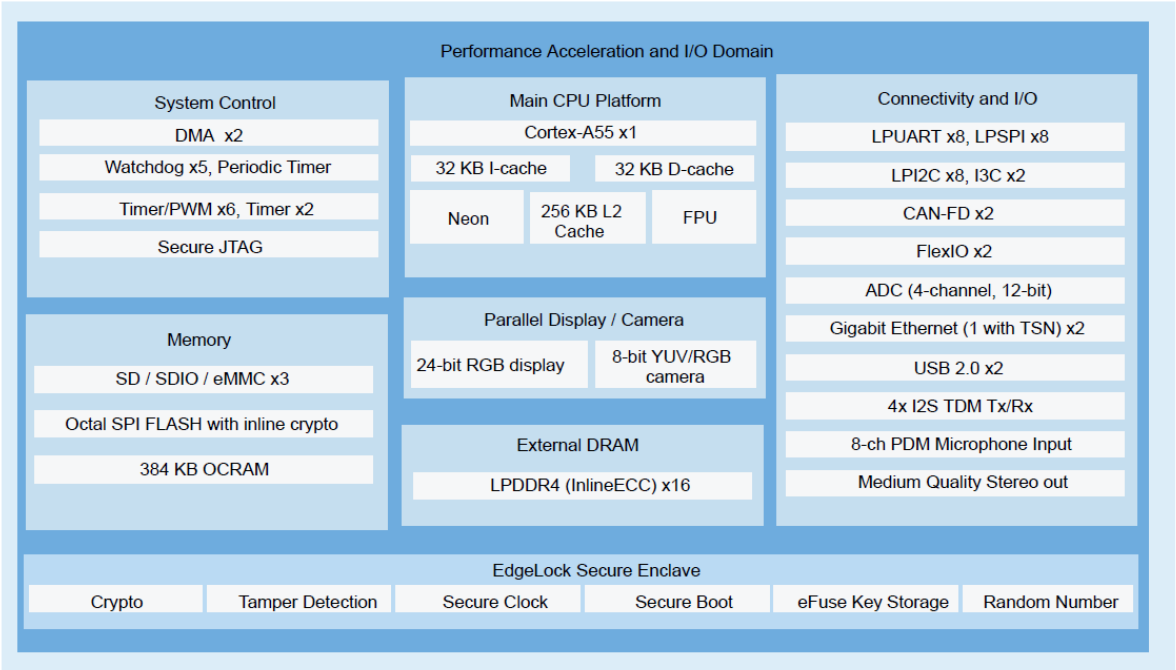
The figures below show block diagrams of the ConnectCore 91 module and of the NXP i.MX 91 application processor.

ConnectCore 91 module



i.MX 91 application processor

Note This is a preliminary diagram.

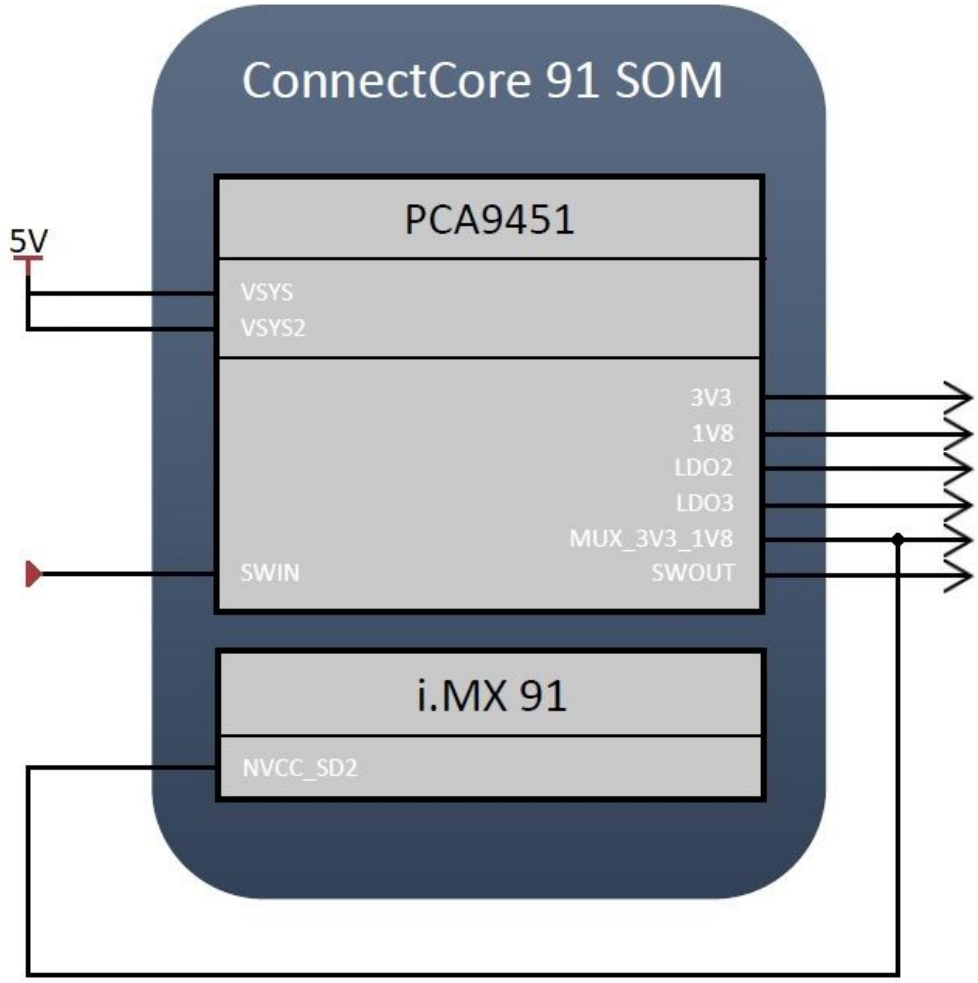


Note The parallel display interface is not available on the ConnectCore 91 module because some of the display interface lines are not exposed in the module connector.

Power interfaces

Reference power diagram

The following diagram represents the power architecture of the ConnectCore 91 module in a typical application:



System-on-module power architecture

The ConnectCore 91 requires two primary power supply inputs: VSYS and VSYS2. These supplies are the input power supplies to the on-module NXP PCA9451 power management IC (PMIC), which generates all required supply voltages for the module as well as the external interfaces.

The following table summarizes the PMIC regulators and switches on the ConnectCore 91 SOM:

PMIC regulator	SOM power rail name	Input power supply	Internally used	Externally available
BUCK1	-	VSYS2	YES	NO
BUCK2	-	VSYS2	YES	NO
BUCK3	-	VSYS2	YES	NO
BUCK4	3V3	VSYS	YES	YES
BUCK5	1V8	VSYS2	YES	YES
BUCK6	-	VSYS2	YES	NO
LDO1	-	VSYS2	YES	NO
LDO4	-	VSYS2	YES	NO
LDO5	MUX_3V3_1V8	VSYS2	NO	YES
Load switch	SWOUT	SWIN	NO	YES

In addition to the input power supplies of the PMIC, other power domains of the SOM must also be set externally. This allows power management flexibility so you can adapt the input voltage of the different interfaces. The following table lists the input power rails that must be powered externally to the SOM together with the devices/power domains they power:

Input rail	Internally connected to	Description
NVCC_SD2	VCC_SD2 pin of the i.MX 91 CPU	IO supply for uSDHC2

Note
MUX_3V3_1V8 (LDO5) output voltage is controlled through SD_VSELECT line:

- SD_VSELECT low (max 0.4 V): LDO5=3.3 V
- SD_VSELECT high (min 1.4 V): LDO5=1.8 V

This regulator can be used to power the NVCC_SD2 power supply of the CPU to automatically adapt the voltage operating level of the interface based on the SDIO speed. For this purpose, connect SD_VSELECT line to SD2_VSELECT (pad AN5) signal of the CPU.

Electrical characteristics

Input power rails

The following table lists the electrical specifications of all input power rails for the ConnectCore 91:

Device	SOM power rail		Input voltage (V)		
			Minimum	Typical	Maximum
PMIC	VSYS		3.7	-	6.0[1]
	VSYS2		2.7	-	6.0[1]
CPU	NVCC_SD2	1.8V mode	1.62	1.80	1.98
		3.3V mode	3.00	3.30	3.465

[1] Absolute maximum ratings.

Output power rails

The following table lists the electrical specifications of all output power rails for the ConnectCore 91:

SOM power rail	Used internally in the SOM	Output voltage			Accuracy (%)		Continuous output current (mA)[1]	Startup time (µs)	
		Min	Typ	Max	Min	Max		Typ	Max
3V3	YES	0.6	-	3.4	-2	2	3000	250	500
1V8	YES	0.6	-	3.4	-2	2	2000	250	500
MUX_3V3_1V8	NO	1.8	-	3.3	-3	3	150	200	-
SWOUT	NO	2.8	-	5.5	-	-	400	200	500

Note Some of the electrical characteristics may depend on the configuration and operation mode of the different regulators. For a complete description of the electrical characteristics of the different output power rails (PMIC regulators), see the PCA9451 datasheet.

[1] The maximum output current involves both external and internal circuitry. For those regulators that are used internally in the SOM, the current available outside will be lower.

Bootstrap

The ConnectCore 91 module can be configured to boot from different devices and interfaces. The boot mode can be selected in two ways:

- Through the boot mode pins (recommended for development).
- Overridden by fuses (recommended for production).

When using the boot mode pins, the boot mode is determined by the binary value stored in the internal BOOT_MODE register. The boot mode is initialized by sampling the BOOT_MODE[3:0] inputs on the rising edge of POR_B. After these inputs are sampled, the subsequent states do not affect BOOT_MODE internal register value.

The BOOT_MODE[3:0] bits are available in the following signals of the SOM:

Signal	Boot mode
BT_UART1_TX	BOOT0
BT_UART1_RTS	BOOT1
SPI1_CS0	BOOT2
SPI1_SCK	BOOT3

Note BT_UART1_RTS (BOOT1) has an internal pull-up to set the module to boot from the on-module eMMC by default.

The following table lists the different boot modes available on the ConnectCore 91 module:

BOOT core	BOOT_MODE[3:0]	Boot mode
Cortex-A55	0000	Internal fuses
	0001	Serial downloader
	0010	USDHC1 8-bit eMMC 5.1
	0011	USDHC2 47-bit SD3.0
	0100	FlexSPI serial NOR
	0101	FlexSPI serial NAND 2K page
	0110	Infinite loop
	0111	Test mode
Cortex-M33	1000	Internal fuses
	1001	Serial downloader
	1010	USDHC1 8-bit eMMC 5.1
	1011	USDHC2 47-bit SD3.0
	1100	FlexSPI serial NOR
	1101	FlexSPI serial NAND 2K page
	1110	Infinite loop
	1111	Test mode

Wireless interfaces

The ConnectCore 91 System-on-module combines a wireless local area network (WLAN) and Bluetooth dual solution to support IEEE802.11 a/b/g/n/ac/ax WLAN standards and Bluetooth 5.4, enabling seamless integration of WLAN/Bluetooth and Low Energy technology. Digi also offers a non-wireless variant of the ConnectCore 91 module.

The following sections include specifications for the wireless interfaces available on the ConnectCore 91 module.

WLAN IEEE 802.11a/b/g/n/ac/ax

The following sections specify the performance of the WLAN IEEE 802.11a/b/g/n/ac/ax interface on the ConnectCore 91 module.

Modulation and data rates

The following table lists modulation values for the ConnectCore 91 module, which supports the following WLAN standards:

Standard	Bandwidth	Guard interval	Data rate (Mbps)							
			1 Mbps	11 Mbps	6 Mbps	54 Mbps	MCS0	MCS7	MCS9	MCS11
802.11b/g/a/n/ac	20 MHz	0.8 us	1	11	6	54	6.5	65		
		0.4 us	1	11	6	54	7.2	72.2		
	40 MHz	0.8 us					13.5	135	180	
		0.4 us					15	150	200	
	80 MHz	0.8 us					29.3	292.5	390	
		0.4 us					32.5	325	433.3	
802.11ax	20 MHz	3.2 us					7.3	73.1	97.5	121.9
		1.6 us					8.1	81.3	108.3	135.4
		0.8 us					8.6	86	114.7	143.4
	40 MHz	3.2 us					14.6	146.3	195	243.8
		1.6 us					16.3	162.5	216.7	270.8
		0.8 us					17.2	172.1	229.4	286.8
	80 MHz	3.2 us					30.6	306.3	408.3	510.4
		1.6 us					34	340.3	453.7	567.1
		0.8 us					36	360.3	480.4	600.5

RF channels

The ConnectCore 91 module supports the following frequency bands:

RF band	Ch. BW	Ch. spacing	Channel number (Center freq. MHz)
2.4 GHz	20 MHz	5 MHz	1(2412), 2(2417), 3(2422), 4(2427), 5(2432), 6(2437), 7(2442), 8(2447), 9(2452), 10(2457), 11(2462), 12(2467), 13(2472), 14 (2484)
	40 MHz	5 MHz	3(2422), 11(2462)
5 GHz	20 MHz	20 MHz	36(5180), 40(5200), 44(5220), 48(5240), 52(5260), 56(5280), 60(5300), 64(5320), 100(5500), 104(5520), 108(5540), 112(5560), 116(5580), 120(5600), 124(5620), 128(5640), 132(5660), 136(5680), 140(5700), 144(5720), 149(5745), 153(5765), 157(5785), 161(5805), 165(5825)
	40 MHz	40 MHz	38(5190), 46(5230), 54(5270), 62(5310), 102(5510), 110(5550), 118(5590), 126(5630), 134(5670), 142(5710), 151(5755), 159 (5795)
	80 MHz	80 MHz	42(5210), 58(5290), 106(5530), 122(5610), 138(5690), 155(5775)

Note Dependent upon regulatory bodies.

2.4 GHz

2.4 GHz band channel #	Center frequency (MHz)	EUROPE (ETSI)	NORTH AMERICA (FCC)	JAPAN
1	2412	✓	✓	✓
2	2417	✓	✓	✓
3	2422	✓	✓	✓

2.4 GHz band channel #	Center frequency (MHz)	EUROPE (ETSI)	NORTH AMERICA (FCC)	JAPAN
4	2427	✓	✓	✓
5	2432	✓	✓	✓
6	2437	✓	✓	✓
7	2442	✓	✓	✓
8	2447	✓	✓	✓
9	2452	✓	✓	✓
10	2457	✓	✓	✓
11	2462	✓	✓	✓
12	2467	✓	No	✓
13	2472	✓	No	✓
14	2484	No	No	802.11b only

5 GHz

5 GHz band channel #	Center frequency (MHz)	EUROPE (ETSI)	NORTH AMERICA (FCC)	JAPAN
36	5180	Indoors	✓	✓
40	5200	Indoors	✓	✓
44	5220	Indoors	✓	✓
48	5240	Indoors	✓	✓
52	5260	Indoors / DFS / TPC	DFS	DFS / TPC
56	5280	Indoors / DFS / TPC	DFS	DFS / TPC

5 GHz band channel #	Center frequency (MHz)	EUROPE (ETSI)	NORTH AMERICA (FCC)	JAPAN
60	5300	Indoors / DFS / TPC	DFS	DFS / TPC
64	5320	Indoors / DFS / TPC	DFS	DFS / TPC
100	5500	DFS / TPC	DFS	DFS / TPC
104	5520	DFS / TPC	DFS	DFS / TPC
108	5540	DFS / TPC	DFS	DFS / TPC
112	5560	DFS / TPC	DFS	DFS / TPC
116	5580	DFS / TPC	DFS	DFS / TPC
120	5600	DFS / TPC	DFS	DFS / TPC
124	5620	DFS / TPC	DFS	DFS / TPC
128	5640	DFS / TPC	DFS	DFS / TPC
132	5660	DFS / TPC	DFS	DFS / TPC
136	5680	DFS / TPC	DFS	DFS / TPC
140	5700	DFS / TPC	DFS	DFS / TPC
149	5745	SRD	✓	No Access
153	5765	SRD	✓	No Access
157	5785	SRD	✓	No Access
161	5805	SRD	✓	No Access
165	5825	SRD	✓	No Access

Note
DFS = Dynamic Frequency Selection
TPC = Transmit Power Control
SRD = Short Range Devices 25 mW max power

Transmit power

The following table lists nominal transmit power values for the ConnectCore 91 module based on NXP IW612 and Murata LBES5PL2EL specifications.

RF band	Standard	Nominal Output power (dBm)
2.4 GHz	802.11b	18 (1 Mbps) - 18 (11 Mbps)
	802.11g	16 (6 Mbps) - 16 (54 Mbps)
	802.11n	16 (MCS0, HT20) - 15 (MCS7, HT20) 16 (MCS0, HT40) - 15 (MCS7, HT40)
	802.11ax	15 (MCS0, HE20) - 13 (MCS11, HE20) 15 (MCS0, HE40) - 13 (MCS11, HE40)
5 GHz	802.11a	16 (6 Mbps) - 16 (54 Mbps)
	802.11n	14 (MCS0, HT20) - 14 (MCS7, HT20) 14 (MCS0, HT40) - 14 (MCS7, HT40)
	802.11ac	14 (MCS0, VHT20) - 14 (MCS8, VHT20) 14 (MCS0, VHT40) - 12 (MCS9, VHT40) 14 (MCS0, VHT80) - 12 (MCS9, VHT80)
	802.11ax	14 (MCS0, HE20) - 10 (MCS11, HE20) 14 (MCS0, HE40) - 10 (MCS11, HE40) 14 (MCS0, HE80) - 10 (MCS11, HE80)

Antenna ports

The ConnectCore 91 module has one antenna port on the module via a dedicated U.FL connector. The antenna port supports WLAN and Bluetooth functionality.

Bluetooth

The ConnectCore 91 module supports both Bluetooth and Bluetooth Low Energy protocols:

- Bluetooth 5.4 with backward-compatibility. Bluetooth class 1 and class 2 transmitter operation.
- Integrated WLAN-Bluetooth coexistence.

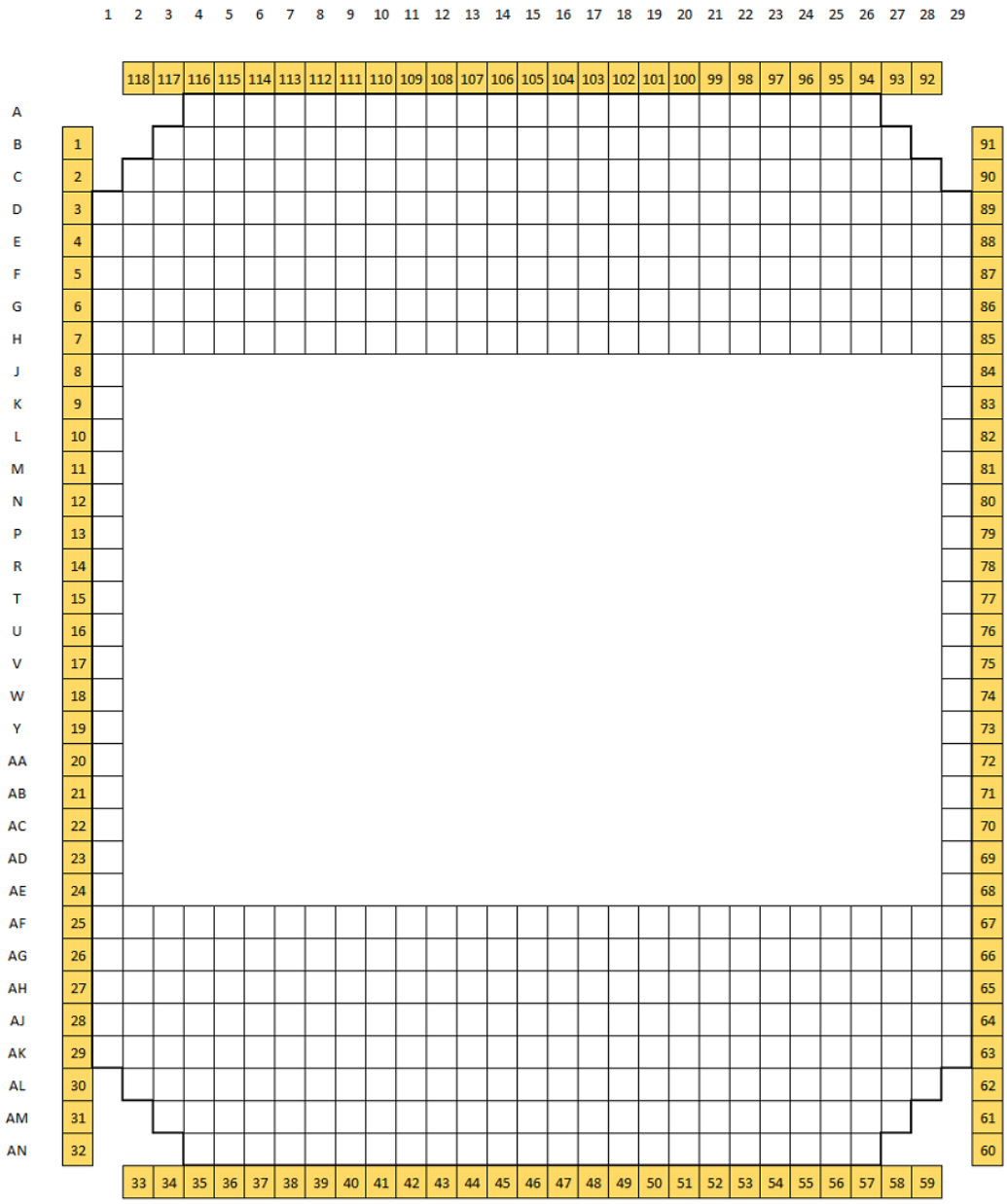
Compatibility within the ConnectCore 9 series

The ConnectCore 93 and the ConnectCore 91 system-on-modules share a common SMTPlus 45x40 form factor. This means that several interfaces are pin-to-pin compatible, enabling you to make a single mother board work for the ConnectCore 9 series of Digi products. Choosing a product with a common form factor enables you to choose a path toward optimized costs, maximum design longevity, and future compatibility without compromising your ability to optimize the board design. You can also leverage common code bases, documentation, and in-house knowledge as your product scales through the product family.

See the ConnectCore 9 compatibility guide in the ConnectCore documentation portal for more information.

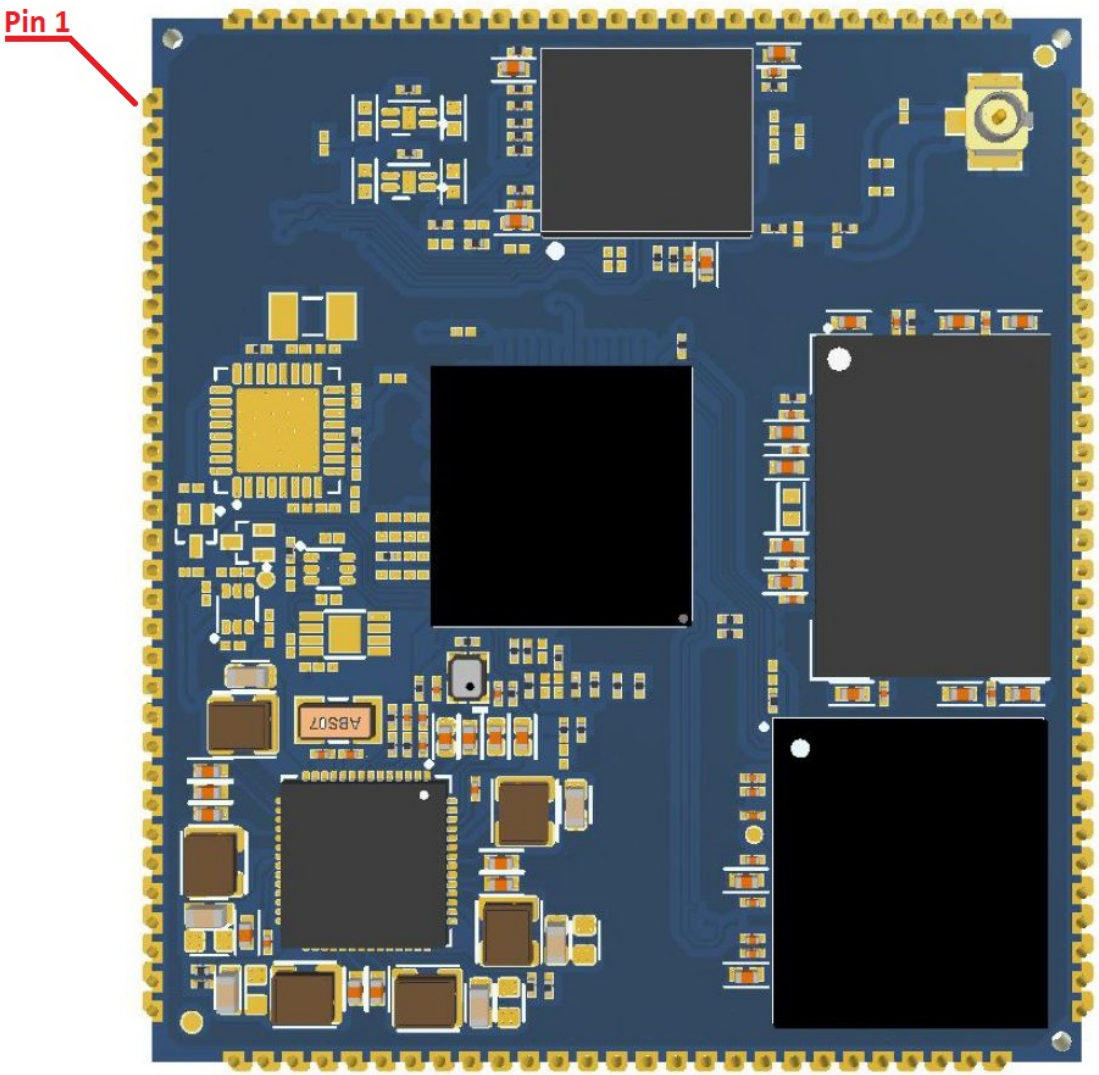
Module pinout

The ConnectCore 91 module has a mixed pad structure. The module provides 474 LGA pins, 118 of them connected to the peripheral castellated pads. The general layout can be found on the following diagram:



White cells: LGA pads
Orange cells: castellated pads

Note The diagram represents the module as seen from the top side with antenna on top-right corner.



External signals and pin multiplexing

The following tables provide the pinout information of the ConnectCore 91 module. For additional information related to the signals listed in the table, refer to the NXP i.MX 91 technical documentation.

Note The Digi ConnectCore Smart IOmux tool can dramatically simplify pin configuration and resolution. You can enter the list of interfaces required by your project and use the Smart IOmux

graphical interface to mock up configuration options, resulting in full pin assignment and device tree snippets that match your desired functionality. See the Smart IOmux User Guide for more information and download instructions.

The microprocessor used on this module, like all CMOS devices, can be driven into a latch-up condition if any I/O pin is driven outside of its associated power rail. Care must be taken to:

- Never drive an I/O pin beyond its positive rail or below ground.
- Never drive an I/O pin from an external power source during the power-on or reset sequences.
- Never hot-swap the module or interrupt its ground connection to external circuitry.

Latch-up is a condition that can cause excessive current draw and result in excessive heating of the microprocessor or its power supplies. This excessive heating can permanently damage the microprocessor and/or its supporting components.

When you use an external supply on the carrier board supporting the ConnectCore 91 module, make sure this supply is NOT back driving i.MX 91 I/Os while their power rails are not enabled. For example, this can happen when an external 3.3V supply is available on the carrier board and this supply powers components driven by i.MX 91 I/Os. In this case, Digi recommends you enable the external power supply after internal 3.3V is enabled, or add the necessary protection circuitry to avoid back voltage (leakage).

Castellated pad signals and multiplexing

Castellated pad number	Associated LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	Multiplexing *(green value represents default functionality)*	Power group	Comments
1	E4	SD2_RESET_B	SD2_RESET_B	**ALT0**: USDHC2_RESET_B **ALT1**: LPTMR2_ALT2 **ALT4**: FLEXIO1_FLEXIO07 **ALT5**: GPIO3_IO07 **ALT6**: CCMSRCGPCMIX_SYSTEM_RESET	NVCC_SD2	
2	E3	GPIO2_IO19	GPIO_IO19	**ALT0**: GPIO2_IO19 **ALT1**: SAI3_RX_SYNC **ALT2**: PDM_BIT_STREAM03 **ALT3**: MEDIAMIX_DISP_DATA15 **ALT4**: LPSPI5_SIN **ALT5**: LPSPI4_SIN **ALT6**: TPM6_CH2 **ALT7**: SAI3_TX_DATA00	3V3	
3	F3	NC				
4	G2	SD2_CD_B	SD2_CD_B	**ALT0**: USDHC2_CD_B **ALT1**: ENET_QOS_1588_EVENT0_IN **ALT2**: I3C2_SCL **ALT3**: LPI2C1_SCL **ALT4**: FLEXIO1_FLEXIO00 **ALT5**: GPIO3_IO00	NVCC_SD2	
5	F1	SD2_CMD	SD2_CMD	**ALT0**: USDHC2_CMD **ALT1**: ENET1_1588_EVENT0_IN **ALT2**: I3C2_PUR **ALT3**: I3C2_PUR_B **ALT4**: FLEXIO1_FLEXIO02 **ALT5**: GPIO3_IO02	NVCC_SD2	

Castellated pad number	Associated LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	Multiplexing *(green value represents default functionality)*	Power group	Comments
6	G1	SD2_DATA0	SD2_DATA0	**ALT0**: USDHC2_DATA0 **ALT1**: ENET2_1588_EVENT0_OUT **ALT2**: CAN2_TX **ALT3**: LPUART1_TX **ALT4**: FLEXIO1_FLEXIO03 **ALT5**: GPIO3_IO03	NVCC_SD2	
7	H1	SD2_DATA1	SD2_DATA1	**ALT0**: USDHC2_DATA1 **ALT1**: ENET2_1588_EVENT1_IN **ALT2**: CAN2_RX **ALT3**: LPUART1_RX **ALT4**: FLEXIO1_FLEXIO04 **ALT5**: GPIO3_IO04	NVCC_SD2	
8	J1	SD2_DATA2	SD2_DATA2	**ALT0**: USDHC2_DATA2 **ALT1**: ENET2_1588_EVENT1_OUT **ALT2**: MQS2_RIGHT **ALT3**: LPUART2_TX **ALT4**: FLEXIO1_FLEXIO05 **ALT5**: GPIO3_IO05	NVCC_SD2	
9	K1	SD2_DATA3	SD2_DATA3	**ALT0**: USDHC2_DATA3 **ALT1**: LPTMR2_ALT1 **ALT2**: MQS2_LEFT **ALT3**: LPUART2_RX **ALT4**: FLEXIO1_FLEXIO06 **ALT5**: GPIO3_IO06	NVCC_SD2	
10	L1	SD2_CLK	SD2_CLK	**ALT0**: USDHC2_CLK **ALT1**: ENET_QOS_1588_EVENT0_OUT **ALT2**: I3C2_SDA **ALT3**: I2C1_SDA **ALT4**: FLEXIO1_FLEXIO01 **ALT5**: GPIO3_IO01	NVCC_SD2	

Castellated pad number	Associated LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	Multiplexing *(green value represents default functionality)*	Power group	Comments
11	M1	GND				
12	N1	NVCC_SD2				
13	P1	UART7_TX	GPIO_IO08	**ALT0**: GPIO2_IO08 **ALT1**: LPSPI3_PCS0 **ALT2**: MEDIAMIX_CAM_DATA02 **ALT3**: MEDIAMIX_DISP_DATA04 **ALT4**: TPM6_CH0 **ALT5**: LPUART7_TX **ALT6**: LPI2C7_SDA **ALT7**: FLEXIO1_FLEXIO08	3V3	
14	R1	UART7_RX	GPIO_IO09	**ALT0**: GPIO2_IO09 **ALT1**: LPSPI3_SIN **ALT2**: MEDIAMIX_CAM_DATA03 **ALT3**: MEDIAMIX_DISP_DATA05 **ALT4**: TPM3_EXTCLK **ALT5**: LPUART7_RX **ALT6**: LPI2C7_SCL **ALT7**: FLEXIO1_FLEXIO09	3V3	
15	T1	GND				
16	U1	NC				
17	V1	I2C2_SCL	I2C2_SCL	**ALT0**: LPI2C2_SCL **ALT1**: I3C1_PUR **ALT2**: LPUART2_DCB_B **ALT3**: TPM2_CH2 **ALT4**: SAI1_RX_SYNC **ALT5**: GPIO1_IO02 **ALT6**: I3C1_PUR_B	3V3	
18	W1	I2C2_SDA	I2C2_SDA	**ALT0**: LPI2C2_SDA **ALT2**: LPUART2_RIN_B	3V3	

Castellated pad number	Associated LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	Multiplexing *(green value represents default functionality)*	Power group	Comments
				ALT3: TPM2_CH3 **ALT4**: SAI1_RX_BCLK **ALT5**: GPIO1_IO03		
19	Y1	GPIO1_IO10	PDM_BIT_STREAM1	**ALT0**: PDM_BIT_STREAM01 **ALT2**: LPSPI2_PCS1 **ALT3**: TPM2_EXTCLK **ALT4**: LPTMR1_ALT3 **ALT5**: GPIO1_IO10	3V3	
20	AA1	GPIO2_IO06	GPIO_IO06	**ALT0**: GPIO2_IO06 **ALT1**: TPM5_CH0 **ALT2**: PDM_BIT_STREAM01 **ALT3**: MEDIAMIX_DISP_DATA02 **ALT4**: LPSPI7_SOUT **ALT5**: LPUART6_CTS_B **ALT6**: LPI2C7_SDA **ALT7**: FLEXIO1_FLEXIO06	3V3	
21	AB1	NC				
22	AC1	NC				
23	AD1	NC				
24	AE1	NC				
25	AF1	GPIO4_IO14 (1V8)	ENET2_MDC	**ALT0**: ENET2_MDC **ALT1**: LPUART4_DCB_B **ALT2**: SAI2_RX_SYNC **ALT4**: FLEXIO2_FLEXIO14 **ALT5**: GPIO4_IO14 **ALT6**: MEDIAMIX_CAM_CLK	1V8	
26	AG1	GPIO4_IO15 (1V8)	ENET2_MDIO	**ALT0**: ENET2_MDIO **ALT1**: LPUART4_RIN_B	1V8	

Castellated pad number	Associated LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	Multiplexing *(green value represents default functionality)*	Power group	Comments
				ALT2: SAI2_RX_BCLK **ALT4**: FLEXIO2_FLEXIO15 **ALT5**: GPIO4_IO15 **ALT6**: MEDIAMIX_CAM_DATA00		
27	AH1	1V8				
28	AJ1	GND				
29	AK1	3V3				
30		GND				
31		VSYS2				
32		VSYS2				
33		VSYS				
34		GND				
35	AN4	GPIO2_IO18	GPIO_IO18	**ALT0**: GPIO2_IO18 **ALT1**: SAI3_RX_BCLK **ALT2**: MEDIAMIX_CAM_DATA09 **ALT3**: MEDIAMIX_DISP_DATA14 **ALT4**: LPSPI5_PCS0 **ALT5**: LPSPI4_PCS0 **ALT6**: TPM5_CH2 **ALT7**: FLEXIO1_FLEXIO18	3V3	
36	AN5	SD2_VSELECT	SD2_VSELECT	**ALT0**: USDHC2_VSELECT **ALT1**: USDHC3_WP **ALT2**: LPTMR2_ALT3 **ALT4**: FLEXIO1_FLEXIO19 **ALT5**: GPIO3_IO19	1V8	
37	AN6	NC				

Castellated pad number	Associated LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	**Multiplexing** *(green value represents default functionality)*	Power group	Comments
38	AN7	NC				
39	AN8	GND				
40	AN9	NC				
41	AN10	NC				
42	AN11	GND				
43	AN12	NC				
44	AN13	NC				
45	AN14	GND				
46	AN15	NC				
47	AN16	NC				
48	AN17	GND				
49	AN18	NC				
50	AN19	NC				
51	AN20	GND				
52	AN21	NC				
53	AN22	NC				
54	AN23	NC				
55	AN24	NC				
56	AN25	SYS_RESET			Internal 1.8 V supply	Reset line of the module (active low

Castellated pad number	Associated LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	Multiplexing *(green value represents default functionality)*	Power group	Comments
						with internal pull-up).
57	AN26	NC				
58	AM27	NC				
59		NC				
60		GND				
61	AL27	NC				
62	AL28	NC				
63	AK29	NC				
64	AJ29	NC				
65	AH29	NC				
66	AG29	NC				
67	AF29	NC				
68	AE29	NC				
69	AD29	NC				
70	AC29	NC				
71	AB29	NC				
72	AA29	NC				
73	Y29	GND				
74	W29	UART6_TX	GPIO_IO04	**ALT0**: GPIO2_IO04 **ALT1**: TPM3_CH0	3V3	

Castellated pad number	Associated LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	Multiplexing *(green value represents default functionality)*	Power group	Comments
				ALT2: PDM_CLK **ALT3**: MEDIAMIX_DISP_DATA00 **ALT4**: LPSPI7_PCS0 **ALT5**: LPUART6_TX **ALT6**: LPI2C6_SDA **ALT7**: FLEXIO1_FLEXIO04		
75	V29	UART6_RX	GPIO_IO05	**ALT0**: GPIO2_IO05 **ALT1**: TPM4_CH0 **ALT2**: PDM_BIT_STREAM00 **ALT3**: MEDIAMIX_DISP_DATA01 **ALT4**: LPSPI7_SIN **ALT5**: LPUART6_RX **ALT6**: LPI2C6_SCL **ALT7**: FLEXIO1_FLEXIO05	3V3	
76	U29	CAN1_RX	PDM_BIT_STREAM0	**ALT0**: PDM_BIT_STREAM00 **ALT1**: MQS1_RIGHT **ALT2**: LPSPI1_PCS1 **ALT3**: TPM1_EXTCLK **ALT4**: LPTMR1_ALT2 **ALT5**: GPIO1_IO09 **ALT6**: CAN1_RX	3V3	
77	T29	CAN1_TX	PDM_CLK	**ALT0**: PDM_CLK **ALT1**: MQS1_LEFT **ALT4**: LPTMR1_ALT1 **ALT5**: GPIO1_IO08 **ALT6**: CAN1_TX	3V3	
78	R29	CAN2_RX	GPIO_IO27	**ALT0**: GPIO2_IO27 **ALT1**: USDHC3_DATA3 **ALT2**: CAN2_RX **ALT3**: MEDIAMIX_DISP_DATA23 **ALT4**: TPM6_CH3	3V3	

Castellated pad number	Associated LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	Multiplexing *(green value represents default functionality)*	Power group	Comments
				ALT5: JTAG_MUX_TMS **ALT6**: LPSPI5_PCS1 **ALT7**: FLEXIO1_FLEXIO27		
79	P29	CAN2_TX	GPIO_IO25	**ALT0**: GPIO2_IO25 **ALT1**: USDHC3_DATA1 **ALT2**: CAN2_TX **ALT3**: MEDIAMIX_DISP_DATA21 **ALT4**: TPM4_CH3 **ALT5**: JTAG_MUX_TCK **ALT6**: LPSPI7_PCS1 **ALT7**: FLEXIO1_FLEXIO25	3V3	
80	N29	UART7_RTS	GPIO_IO11	**ALT0**: GPIO2_IO11 **ALT1**: LPSPI3_SCK **ALT2**: MEDIAMIX_CAM_DATA05 **ALT3**: MEDIAMIX_DISP_DATA07 **ALT4**: TPM5_EXTCLK **ALT5**: LPUART7_RTS_B **ALT6**: LPI2C8_SCL **ALT7**: FLEXIO1_FLEXIO11	3V3	
81	M29	UART7_CTS	GPIO_IO10	**ALT0**: GPIO2_IO10 **ALT1**: LPSPI3_SOUT **ALT2**: MEDIAMIX_CAM_DATA04 **ALT3**: MEDIAMIX_DISP_DATA06 **ALT4**: TPM4_EXTCLK **ALT5**: LPUART7_CTS_B **ALT6**: LPI2C8_SDA **ALT7**: FLEXIO1_FLEXIO10	3V3	
82	L29	ADC_IN1 (1V8)	ADC_IN1			
83	K29	ADC_IN0 (1V8)	ADC_IN0			

Castellated pad number	Associated LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	Multiplexing *(green value represents default functionality)*	Power group	Comments
84	J29	NC				
85	H29	GND				
86	G29	TAMPER0 (1V8)	TAMPER0		Internal 1.8V supply	
87	F29	TAMPER1 (1V8)	TAMPER1		Internal 1.8V supply	
88	E29	I2C4_SDA	GPIO_IO02	**ALT0**: GPIO2_IO02 **ALT1**: LPI2C4_SDA **ALT2**: MEDIAMIX_CAM_VSYNC **ALT3**: MEDIAMIX_DISP_VSYNC **ALT4**: LPSPI6_SOUT **ALT5**: LPUART5_CTS_B **ALT6**: LPI2C6_SDA **ALT7**: FLEXIO1_FLEXIO02	3V3	
89	F28	I2C4_SCL	GPIO_IO03	**ALT0**: GPIO2_IO03 **ALT1**: LPI2C4_SCL **ALT2**: MEDIAMIX_CAM_HSYNC **ALT3**: MEDIAMIX_DISP_HSYNC **ALT4**: LPSPI6_SCK **ALT5**: LPUART5_RTS_B **ALT6**: LPI2C6_SCL **ALT7**: FLEXIO1_FLEXIO03	3V3	
90	E28	GPIO2_IO22	GPIO_IO22	**ALT0**: GPIO2_IO22 **ALT1**: USDHC3_CLK **ALT2**: SPDIF_IN **ALT3**: MEDIAMIX_DISP_DATA18 **ALT4**: TPM5_CH1 **ALT5**: TPM6_EXTCLK **ALT6**: LPI2C5_SDA **ALT7**: FLEXIO1_FLEXIO22	3V3	

Castellated pad number	Associated LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	Multiplexing *(green value represents default functionality)*	Power group	Comments
91	E27	GPIO2_IO23	GPIO_IO23	**ALT0**: GPIO2_IO23 **ALT1**: USDHC3_CMD **ALT2**: SPDIF_OUT **ALT3**: MEDIAMIX_DISP_DATA19 **ALT4**: TPM6_CH1 **ALT6**: LPI2C5_SCL **ALT7**: FLEXIO1_FLEXIO23	3V3	
92	C24	GPIO2_IO24	GPIO_IO24	**ALT0**: GPIO2_IO24 **ALT1**: USDHC3_DATA0 **ALT3**: MEDIAMIX_DISP_DATA20 **ALT4**: TPM3_CH3 **ALT5**: JTAG_MUX_TDO **ALT6**: LPSPI6_PCS1 **ALT7**: FLEXIO1_FLEXIO24	3V3	
93	B24	SAI3_MCLK	GPIO_IO17	**ALT0**: GPIO2_IO17 **ALT1**: SAI3_MCLK **ALT2**: MEDIAMIX_CAM_DATA08 **ALT3**: MEDIAMIX_DISP_DATA13 **ALT4**: LPUART3_RTS_B **ALT5**: LPSPI4_PCS1 **ALT6**: LPUART4_RTS_B **ALT7**: FLEXIO1_FLEXIO17	3V3	
94		GND				
95		NC				
96	A24	ENET1_TXC	ENET1_TXC	**ALT0**: ENET_CCM_QOS_CLOCK_GENERATE_TX_CLK **ALT1**: ENET_QOS_TX_ER **ALT2**: LPSPI2_SIN **ALT4**: FLEXIO2_FLEXIO07 **ALT5**: GPIO4_IO07	1V8	

Castellated pad number	Associated LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	Multiplexing *(green value represents default functionality)*	Power group	Comments
97	A23	ENET1_TX_CTL	ENET1_TX_CTL	**ALT0**: ENET_QOS_RGMII_TX_CTL **ALT1**: LPUART3_DTR_B **ALT2**: LPSPI2_SCK **ALT4**: FLEXIO2_FLEXIO06 **ALT5**: GPIO4_IO06	1V8	
98	A22	ENET1_TXD0	ENET1_TD0	**ALT0**: ENET_QOS_RGMII_TD0 **ALT1**: LPUART3_TX **ALT4**: FLEXIO2_FLEXIO05 **ALT5**: GPIO4_IO05	1V8	
99	A21	ENET1_TXD1	ENET1_TD1	**ALT0**: ENET_QOS_RGMII_TD1 **ALT1**: LPUART3_RTS_B **ALT2**: I3C2_PUR **ALT3**: HSIOMIX_OTG_OC1 **ALT4**: FLEXIO2_FLEXIO04 **ALT5**: GPIO4_IO04 **ALT6**: I3C2_PUR_B	1V8	
100	A20	ENET1_TXD2	ENET1_TD2	**ALT0**: ENET_QOS_RGMII_TD2 **ALT1**: ENET_QOS_CLOCK_GENERATE_REF_CLK **ALT2**: CAN2_RX **ALT3**: HSIOMIX_OTG_OC2 **ALT4**: FLEXIO2_FLEXIO03 **ALT5**: GPIO4_IO03 **ALT6**: LPI2C2_SDA	1V8	
101	A19	ENET1_TXD3	ENET1_TD3	**ALT0**: ENET_QOS_RGMII_TD3 **ALT2**: CAN2_TX **ALT3**: HSIOMIX_OTG_ID2 **ALT4**: FLEXIO2_FLEXIO02 **ALT5**: GPIO4_IO02 **ALT6**: LPI2C2_SCL	1V8	
102	A18	ENET1_RXC	ENET1_RXC	**ALT0**: ENET_QOS_RGMII_RXC	1V8	

Castellated pad number	Associated LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	Multiplexing *(green value represents default functionality)*	Power group	Comments
				ALT1: ENET_QOS_RX_ER **ALT2**: LPSPI2_SOUT **ALT4**: FLEXIO2_FLEXIO09 **ALT5**: GPIO4_IO09		
103	A17	ENET1_RX_CTL	ENET1_RX_CTL	**ALT0**: CCM_ENET_QOS_RGMII_RX_CTL **ALT1**: LPUART3_DSR_B **ALT2**: LPSPI2_PCS0 **ALT3**: HSIOMIX_OTG_PWR2 **ALT4**: FLEXIO2_FLEXIO08 **ALT5**: GPIO4_IO08	1V8	
104	A16	ENET1_RXD0	ENET1_RD0	**ALT0**: ENET_QOS_RGMII_RD0 **ALT1**: LPUART3_RX **ALT4**: FLEXIO2_FLEXIO10 **ALT5**: GPIO4_IO10	1V8	
105	A15	ENET1_RXD1	ENET1_RD1	**ALT0**: ENET_QOS_RGMII_RD1 **ALT1**: LPUART3_CTS_B **ALT3**: LPTMR2_ALT1 **ALT4**: FLEXIO2_FLEXIO11 **ALT5**: GPIO4_IO11	1V8	
106	A14	ENET1_RXD2	ENET1_RD2	**ALT0**: ENET_QOS_RGMII_RD2 **ALT3**: LPTMR2_ALT2 **ALT4**: FLEXIO2_FLEXIO12 **ALT5**: GPIO4_IO12	1V8	
107	A13	ENET1_RXD3	ENET1_RD3	**ALT0**: ENET_QOS_RGMII_RD3 **ALT3**: LPTMR2_ALT3 **ALT4**: FLEXIO2_FLEXIO13 **ALT5**: GPIO4_IO13	1V8	
108	A12	NC				
109	A11	ENET1_MDIO	ENET1_MDIO	**ALT0**: ENET_QOS_MDIO	1V8	

Castellated pad number	Associated LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	Multiplexing *(green value represents default functionality)*	Power group	Comments
				ALT1: LPUART3_RIN_B **ALT2**: I3C2_SDA **ALT3**: HSIOMIX_OTG_PWR1 **ALT4**: FLEXIO2_FLEXIO01 **ALT5**: GPIO4_IO01 **ALT6**: LPI2C1_SDA		
110	A10	ENET1_MDC	ENET1_MDC	**ALT0**: ENET_QOS_MDC **ALT1**: LPUART3_DCB_B **ALT2**: I3C2_SCL **ALT3**: HSIOMIX_OTG_ID1 **ALT4**: FLEXIO2_FLEXIO00 **ALT5**: GPIO4_IO00 **ALT6**: LPI2C1_SCL	1V8	
111	A9	USB_OTG2_P	USB2_D_P			
112	A8	USB_OTG2_N	USB2_D_N			
113	A7	USB_OTG1_P	USB1_D_P			
114	A6	USB_OTG1_N	USB1_D_N			
115		GND				
116	B6	USB1_VBUS	USB1_VBUS			
117	D4	GND				
118	C6	USB_OTG1_ID	USB1_ID		3V3	

LGA signals and multiplexing

LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	**Multiplexing** *(green value represents default functionality)*	Power group	Comments
A4	GND				
A5	GND				
A6	USB_OTG1_N	USB1_D_N			
A7	USB_OTG1_P	USB1_D_P			
A8	USB_OTG2_N	USB2_D_N			
A9	USB_OTG2_P	USB2_D_P			
A10	ENET1_MDC	ENET1_MDC	**ALT0**: ENET_QOS_MDC **ALT1**: LPUART3_DCB_B **ALT2**: I3C2_SCL **ALT3**: HSIOMIX_OTG_ID1 **ALT4**: FLEXIO2_FLEXIO00 **ALT5**: GPIO4_IO00 **ALT6**: LPI2C1_SCL	1V8	
A11	ENET1_MDIO	ENET1_MDIO	**ALT0**: ENET_QOS_MDIO **ALT1**: LPUART3_RIN_B **ALT2**: I3C2_SDA **ALT3**: HSIOMIX_OTG_PWR1 **ALT4**: FLEXIO2_FLEXIO01 **ALT5**: GPIO4_IO01 **ALT6**: LPI2C1_SDA	1V8	
A12	NC				
A13	ENET1_RXD3	ENET1_RD3	**ALT0**: ENET_QOS_RGMII_RD3 **ALT3**: LPTMR2_ALT3	1V8	

LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	Multiplexing *(green value represents default functionality)*	Power group	Comments
			ALT4: FLEXIO2_FLEXIO13 **ALT5**: GPIO4_IO13		
A14	ENET1_RXD2	ENET1_RD2	**ALT0**: ENET_QOS_RGMII_RD2 **ALT3**: LPTMR2_ALT2 **ALT4**: FLEXIO2_FLEXIO12 **ALT5**: GPIO4_IO12	1V8	
A15	ENET1_RXD1	ENET1_RD1	**ALT0**: ENET_QOS_RGMII_RD1 **ALT1**: LPUART3_CTS_B **ALT3**: LPTMR2_ALT1 **ALT4**: FLEXIO2_FLEXIO11 **ALT5**: GPIO4_IO11	1V8	
A16	ENET1_RXD0	ENET1_RD0	**ALT0**: ENET_QOS_RGMII_RD0 **ALT1**: LPUART3_RX **ALT4**: FLEXIO2_FLEXIO10 **ALT5**: GPIO4_IO10	1V8	
A17	ENET1_RX_CTL	ENET1_RX_CTL	**ALT0**: CCM_ENET_QOS_RGMII_RX_CTL **ALT1**: LPUART3_DSR_B **ALT2**: LPSPI2_PCS0 **ALT3**: HSIOMIX_OTG_PWR2 **ALT4**: FLEXIO2_FLEXIO08 **ALT5**: GPIO4_IO08	1V8	
A18	ENET1_RXC	ENET1_RXC	**ALT0**: ENET_QOS_RGMII_RXC **ALT1**: ENET_QOS_RX_ER **ALT2**: LPSPI2_SOUT **ALT4**: FLEXIO2_FLEXIO09 **ALT5**: GPIO4_IO09	1V8	
A19	ENET1_TXD3	ENET1_TD3	**ALT0**: ENET_QOS_RGMII_TD3 **ALT2**: CAN2_TX **ALT3**: HSIOMIX_OTG_ID2 **ALT4**: FLEXIO2_FLEXIO02	1V8	

LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	Multiplexing *(green value represents default functionality)*	Power group	Comments
			ALT5: GPIO4_IO02 **ALT6**: LPI2C2_SCL		
A20	ENET1_TXD2	ENET1_TD2	**ALT0**: ENET_QOS_RGMII_TD2 **ALT1**: ENET_QOS_CLOCK_GENERATE_REF_CLK **ALT2**: CAN2_RX **ALT3**: HSIOMIX_OTG_OC2 **ALT4**: FLEXIO2_FLEXIO03 **ALT5**: GPIO4_IO03 **ALT6**: LPI2C2_SDA	1V8	
A21	ENET1_TXD1	ENET1_TD1	**ALT0**: ENET_QOS_RGMII_TD1 **ALT1**: LPUART3_RTS_B **ALT2**: I3C2_PUR **ALT3**: HSIOMIX_OTG_OC1 **ALT4**: FLEXIO2_FLEXIO04 **ALT5**: GPIO4_IO04 **ALT6**: I3C2_PUR_B	1V8	
A22	ENET1_TXD0	ENET1_TD0	**ALT0**: ENET_QOS_RGMII_TD0 **ALT1**: LPUART3_TX **ALT4**: FLEXIO2_FLEXIO05 **ALT5**: GPIO4_IO05	1V8	
A23	ENET1_TX_CTL	ENET1_TX_CTL	**ALT0**: ENET_QOS_RGMII_TX_CTL **ALT1**: LPUART3_DTR_B **ALT2**: LPSPI2_SCK **ALT4**: FLEXIO2_FLEXIO06 **ALT5**: GPIO4_IO06	1V8	
A24	ENET1_TXC	ENET1_TXC	**ALT0**: ENET_CCM_QOS_CLOCK_GENERATE_TX_CLK **ALT1**: ENET_QOS_TX_ER **ALT2**: LPSPI2_SIN **ALT4**: FLEXIO2_FLEXIO07	1V8	

LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	**Multiplexing** *(green value represents default functionality)*	Power group	Comments
			ALT5: GPIO4_IO07		
A25	GND				
A26	PCM_MCLK				This line comes directly from the Wireless chip. Functionality not supported by default.
B3	GND				
B4	GND				
B5	GND				
B6	USB1_VBUS	USB1_VBUS			
B7	NC				
B8	GND				
B9	NC				
B10	NC				
B11	GND				
B12	NC				
B13	NC				
B14	GND				
B15	GND				

LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	Multiplexing *(green value represents default functionality)*	Power group	Comments
B16	NC				
B17	NC				
B18	GND				
B19	ENET2_TX_CTL	ENET2_TX_CTL	**ALT0**: ENET2_RGMII_TX_CTL **ALT1**: LPUART4_DTR_B **ALT2**: SAI2_TX_SYNC **ALT4**: FLEXIO2_FLEXIO20 **ALT5**: GPIO4_IO20 **ALT6**: MEDIAMIX_CAM_DATA03	1V8	
B20	ENET2_TXC	ENET2_TXC	**ALT0**: ENET2_RGMII_TXC **ALT1**: ENET2_TX_ER **ALT2**: SAI2_TX_BCLK **ALT4**: FLEXIO2_FLEXIO21 **ALT5**: GPIO4_IO21 **ALT6**: MEDIAMIX_CAM_DATA04	1V8	
B21	ENET2_TXD3	ENET2_TD3	**ALT0**: ENET2_RGMII_TD3 **ALT2**: SAI2_RX_DATA00 **ALT4**: FLEXIO2_FLEXIO16 **ALT5**: GPIO4_IO16 **ALT6**: MEDIAMIX_CAM_VSYNC	1V8	
B22	ENET2_RXD3	ENET2_RD3	**ALT0**: ENET2_RGMII_RD3 **ALT1**: SPDIF_OUT **ALT2**: SPDIF_IN **ALT3**: MQS2_LEFT **ALT4**: FLEXIO2_FLEXIO27 **ALT5**: GPIO4_IO27	1V8	
B23	NC				
B24	SAI3_MCLK	GPIO_IO17	**ALT0**: GPIO2_IO17	3V3	

LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	**Multiplexing** *(green value represents default functionality)*	Power group	Comments
			ALT1: SAI3_MCLK **ALT2**: MEDIAMIX_CAM_DATA08 **ALT3**: MEDIAMIX_DISP_DATA13 **ALT4**: LPUART3_RTS_B **ALT5**: LPSPI4_PCS1 **ALT6**: LPUART4_RTS_B **ALT7**: FLEXIO1_FLEXIO17		
B25	GND				
B26	GND				
B27	GND				
C2	GND				
C3	NC				
C4	GND				
C5	GND				
C6	USB_OTG1_ID	USB1_ID		3V3	
C7	NC				
C8	NC				
C9	NC				
C10	USB_OTG2_ID	USB2_ID			
C11	NC				
C12	GND				
C13	GND				

LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	Multiplexing *(green value represents default functionality)*	Power group	Comments
C14	GND				
C15	GND				
C16	GND				
C17	SPI1_CS0	SAI1_TXFS	**ALT0**: SAI1_TX_SYNC **ALT1**: SAI1_TX_DATA01 **ALT2**: LPSPI1_PCS0 **ALT3**: LPUART2_DTR_B **ALT4**: MQS1_LEFT **ALT5**: GPIO1_IO11	3V3	
C18	SPI1_SIN	SAI1_TXC	**ALT0**: SAI1_TX_BCLK **ALT1**: LPUART2_CTS_B **ALT2**: LPSPI1_SIN **ALT3**: LPUART1_DSR_B **ALT4**: CAN1_RX **ALT5**: GPIO1_IO12	3V3	
C19	SAI3_TXFS	GPIO_IO26	**ALT0**: GPIO2_IO26 **ALT1**: USDHC3_DATA2 **ALT2**: PDM_BIT_STREAM01 **ALT3**: MEDIAMIX_DISP_DATA22 **ALT4**: TPM5_CH3 **ALT5**: JTAG_MUX_TDI **ALT6**: LPSPI8_PCS1 **ALT7**: SAI3_TX_SYNC	3V3	
C20	ENET2_RXD2	ENET2_RD2	**ALT0**: ENET2_RGMII_RD2 **ALT1**: LPUART4_CTS_B **ALT2**: SAI2_MCLK **ALT3**: MQS2_RIGHT **ALT4**: FLEXIO2_FLEXIO26 **ALT5**: GPIO4_IO26 **ALT6**: MEDIAMIX_CAM_DATA09	1V8	

LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	Multiplexing *(green value represents default functionality)*	Power group	Comments
C21	ENET2_TXD2	ENET2_TD2	**ALT0**: ENET2_RGMII_TD2 **ALT1**: ENET2_TX_CLK **ALT4**: FLEXIO2_FLEXIO17 **ALT5**: GPIO4_IO17 **ALT6**: MEDIAMIX_CAM_HSYNC	1V8	
C22	ENET2_TXD0	ENET2_TD0	**ALT0**: ENET1_RGMII_TD0 **ALT1**: LPUART4_TX **ALT4**: FLEXIO2_FLEXIO19 **ALT5**: GPIO4_IO19 **ALT6**: MEDIAMIX_CAM_DATA02	1V8	
C23	ENET2_RX_CTL	ENET2_RX_CTL	**ALT0**: ENET2_RGMII_RX_CTL **ALT1**: LPUART4_DSR_B **ALT2**: SAI2_TX_DATA00 **ALT4**: FLEXIO2_FLEXIO22 **ALT5**: GPIO4_IO22 **ALT6**: MEDIAMIX_CAM_DATA05	1V8	
C24	GPIO2_IO24	GPIO_IO24	**ALT0**: GPIO2_IO24 **ALT1**: USDHC3_DATA0 **ALT3**: MEDIAMIX_DISP_DATA20 **ALT4**: TPM3_CH3 **ALT5**: JTAG_MUX_TDO **ALT6**: LPSPI6_PCS1 **ALT7**: FLEXIO1_FLEXIO24	3V3	
C25	GND				
C26	GND				
C27	RF_ANT_EXT				Internal antenna pad.
C28	GND				

LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	Multiplexing *(green value represents default functionality)*	Power group	Comments
D1	NC				
D2	GND				
D3	GND				
D4	GND				
D5	WLAN_SD3_DATA3	SD3_DATA3	**ALT0**: USDHC3_DATA3 **ALT1**: FLEXSPI1_A_DATA03 **ALT2**: LPI2C4_SCL **ALT4**: FLEXIO1_FLEXIO25 **ALT5**: GPIO3_IO25	1V8	This SDIO interface is connected to the Wireless chip on the wireless variants of the SOM. This pads must remain unconnected unless when using a non wireless variant of the module.
D6	WLAN_SD3_DATA2	SD3_DATA2	**ALT0**: USDHC3_DATA2 **ALT1**: FLEXSPI1_A_DATA02 **ALT2**: LPI2C4_SDA **ALT4**: FLEXIO1_FLEXIO24 **ALT5**: GPIO3_IO24	1V8	
D7	NC				
D8	WLAN_SD3_DATA1	SD3_DATA1	**ALT0**: USDHC3_DATA1 **ALT1**: FLEXSPI1_A_DATA01 **ALT2**: LPUART2_RTS_B **ALT4**: FLEXIO1_FLEXIO23 **ALT5**: GPIO3_IO23	1V8	This SDIO interface is connected to the Wireless chip on the wireless variants of the SOM.

LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	Multiplexing *(green value represents default functionality)*	Power group	Comments
					This pads must remain unconnected unless when using a non wireless variant of the module.
D9	WLAN_SD3_DATA0	SD3_DATA0	**ALT0**: USDHC3_DATA0 **ALT1**: FLEXSPI1_A_DATA00 **ALT2**: LPUART2_CTS_B **ALT4**: FLEXIO1_FLEXIO22 **ALT5**: GPIO3_IO22	1V8	
D10	NC				
D11	WLAN_SD3_CMD	SD3_CMD	**ALT0**: USDHC3_CMD **ALT1**: FLEXSPI1_A_SS0_B **ALT2**: LPUART1_RTS_B **ALT4**: FLEXIO1_FLEXIO21 **ALT5**: GPIO3_IO21	1V8	This SDIO interface is connected to the Wireless chip on the wireless variants of the SOM.
D12	WLAN_SD3_CLK	SD3_CLK	**ALT0**: USDHC3_CLK **ALT1**: FLEXSPI1_A_SCLK **ALT2**: LPUART1_CTS_B **ALT4**: FLEXIO1_FLEXIO20 **ALT5**: GPIO3_IO20	1V8	This pads must remain unconnected unless when using a non wireless variant of the module.
D13	NC				
D14	NC				
D15	NC				
D16	GND				

LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	Multiplexing *(green value represents default functionality)*	Power group	Comments
D17	SPI8_SCK	GPIO_IO15	**ALT0**: GPIO2_IO15 **ALT1**: LPUART3_RX **ALT2**: MEDIAMIX_CAM_DATA07 **ALT3**: MEDIAMIX_DISP_DATA11 **ALT4**: LPSPI8_SCK **ALT5**: LPUART8_RTS_B **ALT6**: LPUART4_RX **ALT7**: FLEXIO1_FLEXIO15	3V3	
D18	SPI1_SOUT	SAI1_RXD0	**ALT0**: SAI1_RX_DATA00 **ALT1**: SAI1_MCLK **ALT2**: LPSPI1_SOUT **ALT3**: LPUART2_DSR_B **ALT4**: MQS1_RIGHT **ALT5**: GPIO1_IO14	3V3	
D19	NC				
D20	ENET2_TXD1	ENET2_TD1	**ALT0**: ENET2_RGMII_TD1 **ALT1**: LPUART4_RTS_B **ALT4**: FLEXIO2_FLEXIO18 **ALT5**: GPIO4_IO18 **ALT6**: MEDIAMIX_CAM_DATA01	1V8	
D21	ENET2_RXD0	ENET2_RD0	**ALT0**: ENET2_RGMII_RD0 **ALT1**: LPUART4_RX **ALT4**: FLEXIO2_FLEXIO24 **ALT5**: GPIO4_IO24 **ALT6**: MEDIAMIX_CAM_DATA07	1V8	
D22	ENET2_RXC	ENET2_RXC	**ALT0**: ENET2_RGMII_RXC **ALT1**: ENET2_RX_ER **ALT4**: FLEXIO2_FLEXIO23 **ALT5**: GPIO4_IO23 **ALT6**: MEDIAMIX_CAM_DATA06	1V8	

LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	**Multiplexing** *(green value represents default functionality)*	Power group	Comments
D23	ENET2_RXD1	ENET2_RD1	**ALT0**: ENET2_RGMII_RD1 **ALT1**: SPDIF_IN **ALT4**: FLEXIO2_FLEXIO25 **ALT5**: GPIO4_IO25 **ALT6**: MEDIAMIX_CAM_DATA08	1V8	
D24	GND				
D25	GPIO3_IO27 (1V8)	CCM_CLKO2	**ALT0**: CCMSRCGPCMIX_CLKO2 **ALT4**: FLEXIO1_FLEXIO27 **ALT5**: GPIO3_IO27	Internal 1.8 V supply	
D26	GND				
D27	GND				
D28	GND				
D29	GND				
E1	GND				
E2	GND				
E3	GPIO2_IO19	GPIO_IO19	**ALT0**: GPIO2_IO19 **ALT1**: SAI3_RX_SYNC **ALT2**: PDM_BIT_STREAM03 **ALT3**: MEDIAMIX_DISP_DATA15 **ALT4**: LPSPI5_SIN **ALT5**: LPSPI4_SIN **ALT6**: TPM6_CH2 **ALT7**: SAI3_TX_DATA00	3V3	
E4	SD2_RESET_B	SD2_RESET_B	**ALT0**: USDHC2_RESET_B **ALT1**: LPTMR2_ALT2 **ALT4**: FLEXIO1_FLEXIO07 **ALT5**: GPIO3_IO07	NVCC_ SD2	

LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	Multiplexing *(green value represents default functionality)*	Power group	Comments
			ALT6: CCMSRCGPCMIX_SYSTEM_RESET		
E5	1V8				
E6	GND				
E7	USB2_VBUS	USB2_VBUS			
E8	GND				
E9	IW612_JTAG_TDI				This line comes directly from the Wireless chip. Functionality not supported by default.
E10	IW612_JTAG_TMS				
E11	IW612_JTAG_TCK				
E12	BT_UART1_RXD	UART1_RXD	**ALT0**: LPUART1_RX **ALT1**: ELE_UART_RX **ALT2**: LPSPI2_SIN **ALT3**: TPM1_CH0 **ALT5**: GPIO1_IO04	3V3	Internal UART line used by the Bluetooth. This signal is externally available only in non-wireless variants.
E13	BT_UART1_TXD	UART1_TXD	**ALT0**: LPUART1_TX **ALT1**: ELE_UART_TX **ALT2**: LPSPI2_PCS0 **ALT3**: TPM1_CH1 **ALT5**: GPIO1_IO05	3V3	
E14	SWIN				
E15	GND				
E16	NC				
E17	SPI1_SCK	SAI1_TXD0	**ALT0**: SAI1_TX_DATA00	3V3	

LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	Multiplexing *(green value represents default functionality)*	Power group	Comments
			ALT1: LPUART2_RTS_B **ALT2**: LPSPI1_SCK **ALT3**: LPUART1_DTR_B **ALT4**: CAN1_TX **ALT5**: GPIO1_IO13 **ALT6**: SAI1_MCLK		
E18	SPI8_SOUT	GPIO_IO14	**ALT0**: GPIO2_IO14 **ALT1**: LPUART3_TX **ALT2**: MEDIAMIX_CAM_DATA06 **ALT3**: MEDIAMIX_DISP_DATA10 **ALT4**: LPSPI8_SOUT **ALT5**: LPUART8_CTS_B **ALT6**: LPUART4_TX **ALT7**: FLEXIO1_FLEXIO14	3V3	
E19	SPI8_CS0	GPIO_IO12	**ALT0**: GPIO2_IO12 **ALT1**: TPM3_CH2 **ALT2**: PDM_BIT_STREAM02 **ALT3**: MEDIAMIX_DISP_DATA08 **ALT4**: LPSPI8_PCS0 **ALT5**: LPUART8_TX **ALT6**: LPI2C8_SDA **ALT7**: SAI3_RX_SYNC	3V3	
E20	SAI3_TXD	GPIO_IO21	**ALT0**: GPIO2_IO21 **ALT1**: SAI3_TX_DATA00 **ALT2**: PDM_CLK **ALT3**: MEDIAMIX_DISP_DATA17 **ALT4**: LPSPI5_SCK **ALT5**: LPSPI4_SCK **ALT6**: TPM4_CH1 **ALT7**: SAI3_RX_BCLK	3V3	
E21	SAI3_RXD	GPIO_IO20	**ALT0**: GPIO2_IO20	3V3	

LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	Multiplexing *(green value represents default functionality)*	Power group	Comments
			ALT1: SAI3_RX_DATA00 **ALT2**: PDM_BIT_STREAM00 **ALT3**: MEDIAMIX_DISP_DATA16 **ALT4**: LPSPI5_SOUT **ALT5**: LPSPI4_SOUT **ALT6**: TPM3_CH1 **ALT7**: FLEXIO1_FLEXIO20		
E22	SPI8_SIN	GPIO_IO13	**ALT0**: GPIO2_IO13 **ALT1**: TPM4_CH2 **ALT2**: PDM_BIT_STREAM03 **ALT3**: MEDIAMIX_DISP_DATA09 **ALT4**: LPSPI8_SIN **ALT5**: LPUART8_RX **ALT6**: LPI2C8_SCL **ALT7**: FLEXIO1_FLEXIO13	3V3	
E23	SAI3_TXC	GPIO_IO16	**ALT0**: GPIO2_IO16 **ALT1**: SAI3_TX_BCLK **ALT2**: PDM_BIT_STREAM02 **ALT3**: MEDIAMIX_DISP_DATA12 **ALT4**: LPUART3_CTS_B **ALT5**: LPSPI4_PCS2 **ALT6**: LPUART4_CTS_B **ALT7**: FLEXIO1_FLEXIO16	3V3	
E24	NC				
E25	NC				
E26	NC				
E27	GPIO2_IO23	GPIO_IO23	**ALT0**: GPIO2_IO23 **ALT1**: USDHC3_CMD **ALT2**: SPDIF_OUT **ALT3**: MEDIAMIX_DISP_DATA19	3V3	

LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	Multiplexing *(green value represents default functionality)*	Power group	Comments
			ALT4: TPM6_CH1 **ALT6**: LPI2C5_SCL **ALT7**: FLEXIO1_FLEXIO23		
E28	GPIO2_IO22	GPIO_IO22	**ALT0**: GPIO2_IO22 **ALT1**: USDHC3_CLK **ALT2**: SPDIF_IN **ALT3**: MEDIAMIX_DISP_DATA18 **ALT4**: TPM5_CH1 **ALT5**: TPM6_EXTCLK **ALT6**: LPI2C5_SDA **ALT7**: FLEXIO1_FLEXIO22	3V3	
E29	I2C4_SDA	GPIO_IO02	**ALT0**: GPIO2_IO02 **ALT1**: LPI2C4_SDA **ALT2**: MEDIAMIX_CAM_VSYNC **ALT3**: MEDIAMIX_DISP_VSYNC **ALT4**: LPSPI6_SOUT **ALT5**: LPUART5_CTS_B **ALT6**: LPI2C6_SDA **ALT7**: FLEXIO1_FLEXIO02	3V3	
F1	SD2_CMD	SD2_CMD	**ALT0**: USDHC2_CMD **ALT1**: ENET1_1588_EVENT0_IN **ALT2**: I3C2_PUR **ALT3**: I3C2_PUR_B **ALT4**: FLEXIO1_FLEXIO02 **ALT5**: GPIO3_IO02	NVCC_SD2	
F2	SW_EN				
F3	NC				

LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	Multiplexing *(green value represents default functionality)*	Power group	Comments
F4	15.4_SPI_FRM				This line comes directly from the Wireless chip. Functionality not supported by default.
F5	15.4_SPI_INT				
F6	15.4_SPI_RXD				
F7	15.4_SPI_TXD				
F8	15.4_SPI_CLK				
F9	NC				
F10	NC				
F11	BT_UART1_RTS#	UART2_TXD	**ALT0**: LPUART2_TX **ALT1**: LPUART1_RTS_B **ALT2**: LPSPI2_SCK **ALT3**: TPM1_CH3 **ALT5**: GPIO1_IO07 **ALT7**: SAI3_TX_SYNC	3V3	Internal UART line used by the Bluetooth. This signal is externally available only in non-wireless variants.
F12	BT_UART1_CTS#	UART2_RXD	**ALT0**: LPUART2_RX **ALT1**: LPUART1_CTS_B **ALT2**: LPSPI2_SOUT **ALT3**: TPM1_CH2 **ALT4**: SAI1_MCLK **ALT5**: GPIO1_IO06	3V3	
F13	PCM_OUT				This line comes directly from the Wireless chip. Functionality not supported by default.
F14	PCM_SYNC				

LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	**Multiplexing** *(green value represents default functionality)*	Power group	Comments
F15	GND				
F16	GND				
F17	3V3_RF				
F18	3V3_RF				
F19	NC				
F20	MUX_3V3_1V8				
F21	GND				
F22	GND				
F23	NC				
F24	WL_DEV_WAKE				
F25	NC				
F26	NC				
F27	NC				
F28	I2C4_SCL	GPIO_IO03	**ALT0**: GPIO2_IO03 **ALT1**: LPI2C4_SCL **ALT2**: MEDIAMIX_CAM_HSYNC **ALT3**: MEDIAMIX_DISP_HSYNC **ALT4**: LPSPI6_SCK **ALT5**: LPUART5_RTS_B **ALT6**: LPI2C6_SCL **ALT7**: FLEXIO1_FLEXIO03	3V3	
F29	TAMPER1 (1V8)	TAMPER1		Internal 1.8 V supply	

LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	**Multiplexing** *(green value represents default functionality)*	Power group	Comments
G1	SD2_DATA0	SD2_DATA0	**ALT0**: USDHC2_DATA0 **ALT1**: ENET2_1588_EVENT0_OUT **ALT2**: CAN2_TX **ALT3**: LPUART1_TX **ALT4**: FLEXIO1_FLEXIO03 **ALT5**: GPIO3_IO03	NVCC_SD2	
G2	SD2_CD_B	SD2_CD_B	**ALT0**: USDHC2_CD_B **ALT1**: ENET_QOS_1588_EVENT0_IN **ALT2**: I3C2_SCL **ALT3**: LPI2C1_SCL **ALT4**: FLEXIO1_FLEXIO00 **ALT5**: GPIO3_IO00	NVCC_SD2	
G3	NC				
G4	NC				
G5	GND				
G6	NC				
G7	NC				
G8	GND				
G9	NC				
G10	NC				
G11	GND				
G12	BT_DEV_WAKE				

LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	**Multiplexing** *(green value represents default functionality)*	Power group	Comments
G13	PCM_CLK				This line comes directly from the Wireless chip. Functionality not supported by default.
G14	PCM_IN				
G15	IW612_JTAG_TDO				
G16	GND				
G17	BT_HOST_WAKE				
G18	WL_HOST_WAKE				
G19	GND				
G20	NC				
G21	NC				
G22	GND				
G23	NC				
G24	NC				
G25	GND				
G26	GND				
G27	GND				
G28	GND				
G29	TAMPER0 (1V8)	TAMPER0		Internal 1.8 V supply	

LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	Multiplexing *(green value represents default functionality)*	Power group	Comments
H1	SD2_DATA1	SD2_DATA1	**ALT0**: USDHC2_DATA1 **ALT1**: ENET2_1588_EVENT1_IN **ALT2**: CAN2_RX **ALT3**: LPUART1_RX **ALT4**: FLEXIO1_FLEXIO04 **ALT5**: GPIO3_IO04	NVCC_ SD2	
H2	GND				
H3	GND				
H4	GND				
H5	GND				
H6	GND				
H7	GND				
H8	GND				
H9	GND				
H10	GND				
H11	GND				
H12	GND				
H13	GND				
H14	GND				
H15	GND				
H16	GND				
H17	GND				

LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	**Multiplexing** *(green value represents default functionality)*	Power group	Comments
H18	GND				
H19	GND				
H20	GND				
H21	GND				
H22	GND				
H23	GND				
H24	GND				
H25	GND				
H26	GND				
H27	GND				
H28	GND				
H29	GND				
J1	SD2_DATA2	SD2_DATA2	**ALT0**: USDHC2_DATA2 **ALT1**: ENET2_1588_EVENT1_OUT **ALT2**: MQS2_RIGHT **ALT3**: LPUART2_TX **ALT4**: FLEXIO1_FLEXIO05 **ALT5**: GPIO3_IO05	NVCC_ SD2	
J29	NC				
K1	SD2_DATA3	SD2_DATA3	**ALT0**: USDHC2_DATA3 **ALT1**: LPTMR2_ALT1 **ALT2**: MQS2_LEFT **ALT3**: LPUART2_RX **ALT4**: FLEXIO1_FLEXIO06	NVCC_ SD2	

LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	Multiplexing *(green value represents default functionality)*	Power group	Comments
			ALT5: GPIO3_IO06		
K29	ADC_IN0 (1V8)	ADC_IN0			
L1	SD2_CLK	SD2_CLK	**ALT0**: USDHC2_CLK **ALT1**: ENET_QOS_1588_EVENT0_OUT **ALT2**: I3C2_SDA **ALT3**: I2C1_SDA **ALT4**: FLEXIO1_FLEXIO01 **ALT5**: GPIO3_IO01	NVCC_ SD2	
L29	ADC_IN1 (1V8)	ADC_IN1			
M1	GND				
M29	UART7_CTS	GPIO_IO10	**ALT0**: GPIO2_IO10 **ALT1**: LPSPI3_SOUT **ALT2**: MEDIAMIX_CAM_DATA04 **ALT3**: MEDIAMIX_DISP_DATA06 **ALT4**: TPM4_EXTCLK **ALT5**: LPUART7_CTS_B **ALT6**: LPI2C8_SDA **ALT7**: FLEXIO1_FLEXIO10	3V3	
N1	NVCC_SD2				
N29	UART7_RTS	GPIO_IO11	**ALT0**: GPIO2_IO11 **ALT1**: LPSPI3_SCK **ALT2**: MEDIAMIX_CAM_DATA05 **ALT3**: MEDIAMIX_DISP_DATA07 **ALT4**: TPM5_EXTCLK **ALT5**: LPUART7_RTS_B **ALT6**: LPI2C8_SCL **ALT7**: FLEXIO1_FLEXIO11	3V3	
P1	UART7_TX	GPIO_IO08	**ALT0**: GPIO2_IO08	3V3	

LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	**Multiplexing** *(green value represents default functionality)*	Power group	Comments
			ALT1: LPSPI3_PCS0 **ALT2**: MEDIAMIX_CAM_DATA02 **ALT3**: MEDIAMIX_DISP_DATA04 **ALT4**: TPM6_CH0 **ALT5**: LPUART7_TX **ALT6**: LPI2C7_SDA **ALT7**: FLEXIO1_FLEXIO08		
P29	CAN2_TX	GPIO_IO25	**ALT0**: GPIO2_IO25 **ALT1**: USDHC3_DATA1 **ALT2**: CAN2_TX **ALT3**: MEDIAMIX_DISP_DATA21 **ALT4**: TPM4_CH3 **ALT5**: JTAG_MUX_TCK **ALT6**: LPSPI7_PCS1 **ALT7**: FLEXIO1_FLEXIO25	3V3	
R1	UART7_RX	GPIO_IO09	**ALT0**: GPIO2_IO09 **ALT1**: LPSPI3_SIN **ALT2**: MEDIAMIX_CAM_DATA03 **ALT3**: MEDIAMIX_DISP_DATA05 **ALT4**: TPM3_EXTCLK **ALT5**: LPUART7_RX **ALT6**: LPI2C7_SCL **ALT7**: FLEXIO1_FLEXIO09	3V3	
R29	CAN2_RX	GPIO_IO27	**ALT0**: GPIO2_IO27 **ALT1**: USDHC3_DATA3 **ALT2**: CAN2_RX **ALT3**: MEDIAMIX_DISP_DATA23 **ALT4**: TPM6_CH3 **ALT5**: JTAG_MUX_TMS **ALT6**: LPSPI5_PCS1 **ALT7**: FLEXIO1_FLEXIO27	3V3	

LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	Multiplexing *(green value represents default functionality)*	Power group	Comments
T1	GND				
T29	CAN1_TX	PDM_CLK	**ALT0**: PDM_CLK **ALT1**: MQS1_LEFT **ALT4**: LPTMR1_ALT1 **ALT5**: GPIO1_IO08 **ALT6**: CAN1_TX	3V3	
U1	NC				
U29	CAN1_RX	PDM_BIT_STREAM0	**ALT0**: PDM_BIT_STREAM00 **ALT1**: MQS1_RIGHT **ALT2**: LPSPI1_PCS1 **ALT3**: TPM1_EXTCLK **ALT4**: LPTMR1_ALT2 **ALT5**: GPIO1_IO09 **ALT6**: CAN1_RX	3V3	
V1	I2C2_SCL	I2C2_SCL	**ALT0**: LPI2C2_SCL **ALT1**: I3C1_PUR **ALT2**: LPUART2_DCB_B **ALT3**: TPM2_CH2 **ALT4**: SAI1_RX_SYNC **ALT5**: GPIO1_IO02 **ALT6**: I3C1_PUR_B	3V3	
V29	UART6_RX	GPIO_IO05	**ALT0**: GPIO2_IO05 **ALT1**: TPM4_CH0 **ALT2**: PDM_BIT_STREAM00 **ALT3**: MEDIAMIX_DISP_DATA01 **ALT4**: LPSPI7_SIN **ALT5**: LPUART6_RX **ALT6**: LPI2C6_SCL **ALT7**: FLEXIO1_FLEXIO05	3V3	
W1	I2C2_SDA	I2C2_SDA	**ALT0**: LPI2C2_SDA	3V3	

LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	**Multiplexing** *(green value represents default functionality)*	Power group	Comments
			ALT2: LPUART2_RIN_B **ALT3**: TPM2_CH3 **ALT4**: SAI1_RX_BCLK **ALT5**: GPIO1_IO03		
W29	UART6_TX	GPIO_IO04	**ALT0**: GPIO2_IO04 **ALT1**: TPM3_CH0 **ALT2**: PDM_CLK **ALT3**: MEDIAMIX_DISP_DATA00 **ALT4**: LPSPI7_PCS0 **ALT5**: LPUART6_TX **ALT6**: LPI2C6_SDA **ALT7**: FLEXIO1_FLEXIO04	3V3	
Y1	GPIO1_IO10	PDM_BIT_STREAM1	**ALT0**: PDM_BIT_STREAM01 **ALT2**: LPSPI2_PCS1 **ALT3**: TPM2_EXTCLK **ALT4**: LPTMR1_ALT3 **ALT5**: GPIO1_IO10	3V3	
Y29	GND				
AA1	GPIO2_IO06	GPIO_IO06	**ALT0**: GPIO2_IO06 **ALT1**: TPM5_CH0 **ALT2**: PDM_BIT_STREAM01 **ALT3**: MEDIAMIX_DISP_DATA02 **ALT4**: LPSPI7_SOUT **ALT5**: LPUART6_CTS_B **ALT6**: LPI2C7_SDA **ALT7**: FLEXIO1_FLEXIO06	3V3	
AA29	NC				
AB1	NC				
AB29	NC				

LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	Multiplexing *(green value represents default functionality)*	Power group	Comments
AC1	NC				
AC29	NC				
AD1	NC				
AD29	NC				
AE1	NC				
AE29	NC				
AF1	GPIO4_IO14 (1V8)	ENET2_MDC	**ALT0**: ENET2_MDC **ALT1**: LPUART4_DCB_B **ALT2**: SAI2_RX_SYNC **ALT4**: FLEXIO2_FLEXIO14 **ALT5**: GPIO4_IO14 **ALT6**: MEDIAMIX_CAM_CLK	1V8	
AF2	GND				
AF3	GND				
AF4	GND				
AF5	GND				
AF6	GND				
AF7	GND				
AF8	GND				
AF9	GND				
AF10	GND				
AF11	GND				

LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	**Multiplexing** *(green value represents default functionality)*	Power group	Comments
AF12	GND				
AF13	GND				
AF14	GND				
AF15	GND				
AF16	GND				
AF17	GND				
AF18	GND				
AF19	GND				
AF20	GND				
AF21	GND				
AF22	GND				
AF23	GND				
AF24	GND				
AF25	GND				
AF26	GND				
AF27	GND				
AF28	GND				
AF29	NC				
AG1	GPIO4_IO15 (1V8)	ENET2_MDIO	**ALT0**: ENET2_MDIO **ALT1**: LPUART4_RIN_B **ALT2**: SAI2_RX_BCLK	1V8	

LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	Multiplexing *(green value represents default functionality)*	Power group	Comments
			ALT4: FLEXIO2_FLEXIO15 **ALT5**: GPIO4_IO15 **ALT6**: MEDIAMIX_CAM_DATA00		
AG2	GND				
AG3	GND				
AG4	GND				
AG5	GND				
AG6	GND				
AG7	GND				
AG8	NC				
AG9	NC				
AG10	NC				
AG11	NC				
AG12	NC				
AG13	NC				
AG14	NC				
AG15	NC				
AG16	GND				
AG17	SWOUT				
AG18	ON_OFF	ONOFF		Internal 1.8 V supply	ON/OFF signal from the CPU (active low

LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	**Multiplexing** *(green value represents default functionality)*	Power group	Comments
					with internal pull-up).
AG19	NC				
AG20	JTAG_TCK	JTAG_TCK			
AG21	JTAG_TDO	JTAG_TDO			
AG22	NC				
AG23	GND				
AG24	NC				
AG25	GPIO4_IO28 (1V8)	CCM_CLKO3	**ALT0**: CCMSRCGPCMIX_CLKO3 **ALT4**: FLEXIO2_FLEXIO28 **ALT5**: GPIO4_IO28	Internal 1.8 V supply	
AG26	ADC_IN3 (1V8)	ADC_IN3			
AG27	ADC_IN2 (1V8)	ADC_IN2			
AG28	GPIO4_IO29 (1V8)	CCM_CLKO4	**ALT0**: CCMSRCGPCMIX_CLKO4 **ALT4**: FLEXIO2_FLEXIO29 **ALT5**: GPIO4_IO29	Internal 1.8 V supply	
AG29	NC				
AH1	1V8				
AH2	1V8				
AH3	1V8				
AH4	GND				
AH5	GND				

LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	**Multiplexing** *(green value represents default functionality)*	Power group	Comments
AH6	RESERVED				
AH7	NC				
AH8	GND				
AH9	NC				
AH10	POR_B	POR_B			
AH11	NC				
AH12	RESERVED				
AH13	SD_VSELECT				
AH14	GND				
AH15	NC				
AH16	NC				
AH17	GND				
AH18	NC				
AH19	GND				
AH20	NC				
AH21	GND				
AH22	NC				
AH23	NC				
AH24	NC				
AH25	NC				

LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	Multiplexing *(green value represents default functionality)*	Power group	Comments
AH26	NC				
AH27	JTAG_TDI				
AH28	JTAG_TMS				
AH29	NC				
AJ1	GND				
AJ2	VSYS2				
AJ3	VSYS2				
AJ4	VSYS2				
AJ5	GND				
AJ6	GND				
AJ7	GND				
AJ8	NC				
AJ9	GND				
AJ10	NC				
AJ11	PMIC_STANDBY				
AJ12	PWR_ON				
AJ13	NC				
AJ14	GND				
AJ15	NC				
AJ16	NC				

LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	**Multiplexing** *(green value represents default functionality)*	Power group	Comments
AJ17	GND				
AJ18	NC				
AJ19	NC				
AJ20	GND				
AJ21	NC				
AJ22	NC				
AJ23	NC				
AJ24	NC				
AJ25	NC				
AJ26	GND				
AJ27	NC				
AJ28	NC				
AJ29	NC				
AK1	3V3				
AK2	VSYS2				
AK3	VSYS2				
AK4	VSYS2				
AK5	GND				
AK6	GND				
AK7	GND				

LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	**Multiplexing** *(green value represents default functionality)*	Power group	Comments
AK8	GND				
AK9	GND				
AK10	GND				
AK11	GND				
AK12	GND				
AK13	GND				
AK14	GND				
AK15	NC				
AK16	NC				
AK17	GND				
AK18	NC				
AK19	NC				
AK20	GND				
AK21	NC				
AK22	NC				
AK23	GND				
AK24	I2C3_SDA	GPIO_IO00	**ALT0**: GPIO2_IO00 **ALT1**: LPI2C3_SDA **ALT2**: MEDIAMIX_CAM_CLK **ALT3**: MEDIAMIX_DISP_CLK **ALT4**: LPSPI6_PCS0 **ALT5**: LPUART5_TX **ALT6**: LPI2C5_SDA	3V3	

LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	**Multiplexing** *(green value represents default functionality)*	Power group	Comments
			ALT7: FLEXIO1_FLEXIO00		
AK25	I2C3_SCL	GPIO_IO01	**ALT0**: GPIO2_IO01 **ALT1**: LPI2C3_SCL **ALT2**: MEDIAMIX_CAM_DATA00 **ALT3**: MEDIAMIX_DISP_DE **ALT4**: LPSPI6_SIN **ALT5**: LPUART5_RX **ALT6**: LPI2C5_SCL **ALT7**: FLEXIO1_FLEXIO01	3V3	
AK26	NC				
AK27	NC				
AK28	NC				
AK29	NC				
AL2	3V3				
AL3	3V3				
AL4	GND				
AL5	GND				
AL6	VSYS				
AL7	VSYS				
AL8	VSYS				
AL9	GND				
AL10	GND				
AL11	GND				

LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	Multiplexing *(green value represents default functionality)*	Power group	Comments
AL12	NC				
AL13	NC				
AL14	GND				
AL15	NC				
AL16	NC				
AL17	GND				
AL18	GPIO3_IO26 (1V8)	CCM_CLKO1	**ALT0**: CCMSRCGPCMIX_CLKO1 **ALT4**: FLEXIO1_FLEXIO26 **ALT5**: GPIO3_IO26	Internal 1.8 V supply	Internal pull-up.
AL19	RESERVED				
AL20	RESERVED				
AL21	NC				
AL22	NC				
AL23	NC				
AL24	NC				
AL25	NC				
AL26	NC				
AL27	NC				
AL28	NC				
AM3	3V3				

LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	**Multiplexing** *(green value represents default functionality)*	Power group	Comments
AM4	3V3				
AM5	GND				
AM6	GND				
AM7	NC				
AM8	NC				
AM9	NC				
AM10	CLKIN1				
AM11	CLKIN2				
AM12	GND				
AM13	NC				
AM14	NC				
AM15	GND				
AM16	NC				
AM17	NC				
AM18	GND				
AM19	RESERVED				
AM20	GND				
AM21	NC				
AM22	RESERVED				
AM23	NC				

LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	Multiplexing *(green value represents default functionality)*	Power group	Comments
AM24	NC				
AM25	NC				
AM26	NC				
AM27	NC				
AN4	GPIO2_IO18	GPIO_IO18	**ALT0**: GPIO2_IO18 **ALT1**: SAI3_RX_BCLK **ALT2**: MEDIAMIX_CAM_DATA09 **ALT3**: MEDIAMIX_DISP_DATA14 **ALT4**: LPSPI5_PCS0 **ALT5**: LPSPI4_PCS0 **ALT6**: TPM5_CH2 **ALT7**: FLEXIO1_FLEXIO18	3V3	
AN5	SD2_VSELECT	SD2_VSELECT	**ALT0**: USDHC2_VSELECT **ALT1**: USDHC3_WP **ALT2**: LPTMR2_ALT3 **ALT4**: FLEXIO1_FLEXIO19 **ALT5**: GPIO3_IO19	1V8	
AN6	NC				
AN7	NC				
AN8	GND				
AN9	NC				
AN10	NC				
AN11	GND				
AN12	NC				

LGA pad name	ConnectCore 91 signal name	i.MX 91 pin name	**Multiplexing** *(green value represents default functionality)*	Power group	Comments
AN13	NC				
AN14	GND				
AN15	NC				
AN16	NC				
AN17	GND				
AN18	NC				
AN19	NC				
AN20	GND				
AN21	NC				
AN22	NC				
AN23	NC				
AN24	NC				
AN25	SYS_RESET			Internal 1.8 V supply	Reset line of the module (active low with internal pull-up).
AN26	NC				

Module specifications

The following sections describe the specifications for the ConnectCore 91 SOM.

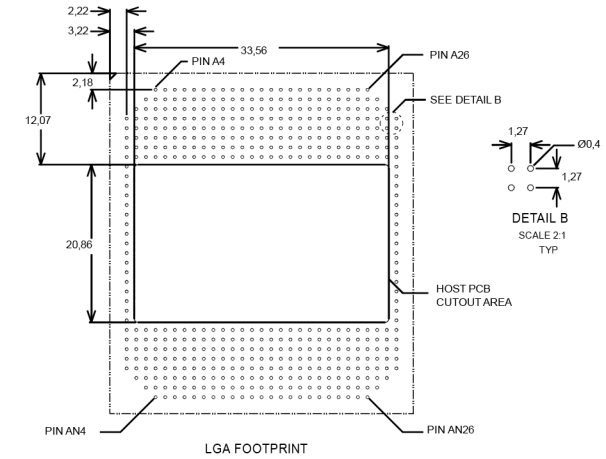
Power consumption 82
Mechanical specifications 82

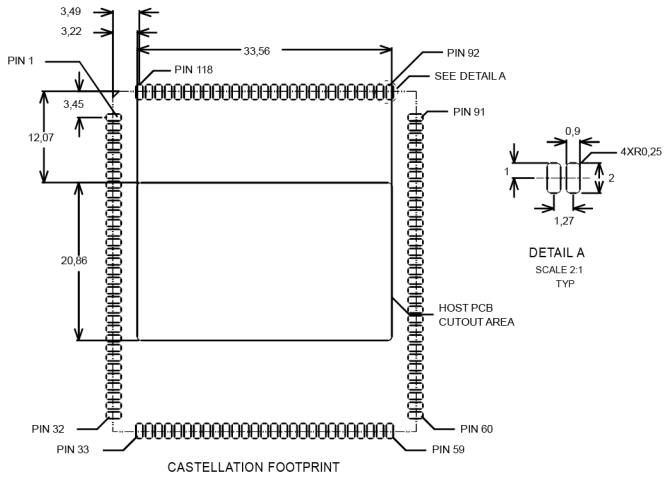
Power consumption

For information on the power consumption of the ConnectCore 91, refer to the ConnectCore 91 Performance and Power Benchmarking Report.

Mechanical specifications

Host PCB footprint and cutout





Label

The MAC address and serial number of the SOM are encoded in the data matrix on the SOM label.

Weight

The weight of the ConnectCore 91 module is 9.6 g.

Note See the ConnectCore 91 support page for links to vector files, additional mechanical drawings, and other design documents.

Environmental specifications

Operating temperature: -40 to 85 °C.

CAUTION! Your final product may require additional thermal management such as passive (heatsink/spreader) or active (airflow) cooling to achieve the maximum operating temperature without exceeding the processor junction temp limit.

Socket options

For testing, prototyping, and other primarily development-related purposes, Digi International and E-tec Interconnect AG have developed sockets allowing the easy insertion and removal of modules in a carrier board design.

All drawings, user instructions, schematics and PCB footprints are posted on the ConnectCore 91 technical support website.

Note The ConnectCore 91 Development Board (Digi P/N CC-WMX93-KIT) has been designed to support a LPF474-129M-32ACEW55L socket, and can be used as a reference design.

All sockets are sold and built by E-tec Interconnect AG. The table below provides an overview of the available part numbers.

Socket model	E-tec part number
ConnectCore 91 Castellated	LPQ118-1290-32AAEW55L rev1
ConnectCore 91 LGA	LPF474-129M-32ACEW55L rev1

Note Please direct all socket-related purchase inquiries to E-tec Interconnect AG (info@e-tec.com).

MTBF

MTBF (Mean Time Before Failure) has been estimate using the method of prediction Telcordia Reliability Prediction Procedure, SR-332, Issue 4, “Parts Count” Method.

The following assumptions have been made:

- An average ambient temperature of +23°C.
- Electrical Stress of 50%
- Quality Level II for all components
- Mission profile considered in this analysis is a yearly continuous operation i.e. always operating On, 365 days per year.
- Average module temperature rise = 17°C
- Two different environmental factors have been considered:
- An environmental factor of π~E~ = 1.2 is defined in SR-332 for Ground, Fixed, Uncontrolled (limited) environments (GL).

- An environmental factor of π~E~ = 2 is defined in SR-332 for Ground, Mobile environments (GM).

Product variant	Ground fixed, Uncontrolled (limited) – MTTF (hours)	Ground Mobile – MTTF (hours)
ConnectCore 91 wireless	4 424 779	2 652 520
ConnectCore 91 non-wireless	4 854 369	2 915 452

Failure rate and MTTF (Mean Time To Failure) for different operational temperature:

Operating temperature (°C)	25	36	40	50	60
ConnectCore 91 wireless	5 847 953	4 975 124	4 424 779	3 215 434	2 277 904
ConnectCore 91 non-wireless	6 410 256	5 464 481	4 854 369	3 546 099	2 518 892

Note Values above assume MTTF Ground Fixed, Uncontrolled (limited) x1.2 environment.
Other environmental stresses lower MTTF values.

Assembly instructions

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Reflow oven profile 88

Moisture sensitivity and shelf life

The ConnectCore 91 is classified as a Level 3 Moisture Sensitive Device in accordance with IPC/JEDEC J-STD-020.

1. Calculated shelf life in sealed packaging: 12 months at <40°C and <90% relative humidity (RH).
2. Environmental condition during production: 30°C / 60% RH according to IPC/JEDEC J-STD-033C paragraph 5.
3. After module is removed from sealed packaging, modules that will be subjected to reflow solder temperatures are required to be:
   a. Mounted within 168 hours.
   b. Stored per J-STD-033.
4. Baking is required, before mounting if:
   a. the packaging humidity indicator indicates 10% RH or higher.
   b. either 3a or 3b are not met.
5. If baking is required, bake modules in trays for 4-6 hours at 125°C; maximum stacking height is 10 trays.

Mounting

The ConnectCore 91 has been designed with easy integration into existing SMT processes in mind. This section contains guidance for mounting the module on your carrier board.

The module can be configured and mounted in a Castellation OR Land Grid Array (LGA) form.

Modules are not sealed and therefore they should not be subjected to a wash cycle or similar treatment where condensation could occur.

Coplanarity

The coplanarity measured is <0.003" bow and twist (98% confidence interval). It is important that the carrier board is also coplanar. It is recommended that the assembly be supported during the reflow process with a fixture to minimize the potential bow of the carrier card.

Stencil

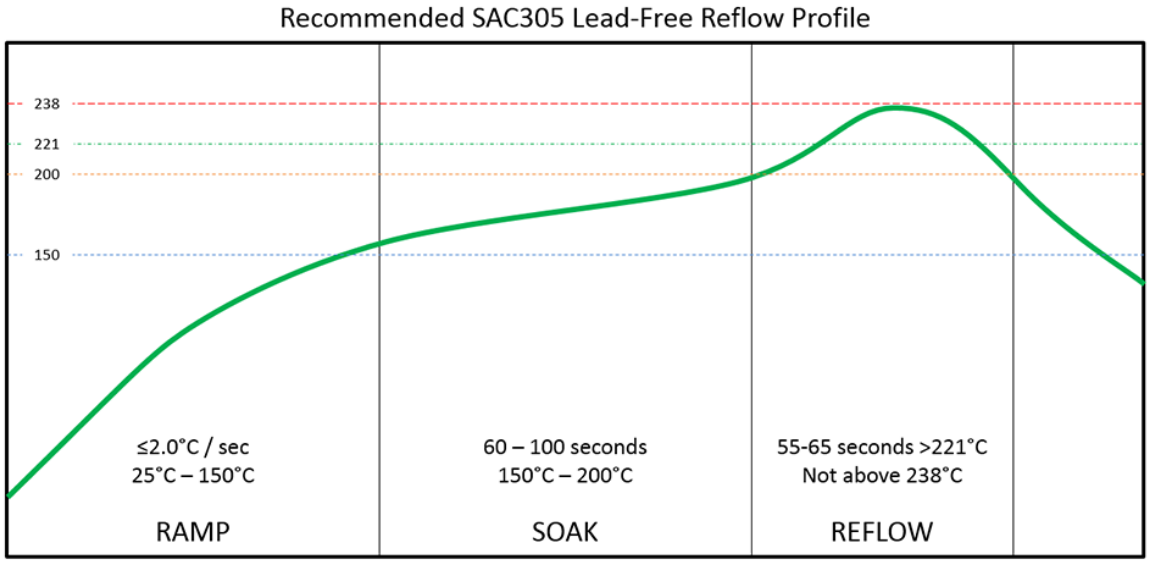
For both castellation AND LGA applications, Digi recommends a laser cut and/or electro- formed stencil. Based on the actual coplanarity characteristics of your carrier board, adjustments may be required to determine the optimal solder paste volume.

SMT process parameter reference - Castellation and LGA applications

Process	SMT process	Specification recommendations
Screen Print	Solder paste	SAC 305 No-Clean (Alpha OM-340 or equivalent)
	Stencil thickness	0.100 mm / 4mil
	Recommended aperture size	LGA – 0.4 to 0.5 mm circle or rounded square Castellation – 1:1 with pad size
	Paste alignment	20% maximum off center of the pad
PnP	Placement nozzle	Largest available on machine
	Nozzle pick surface	Module center
	Speed	Slowest possible with PnP machine
	Placement sequence	Last, if possible
	Placement alignment	10% maximum off center of pad
Reflow	See Reflow oven profile.	

Reflow oven profile

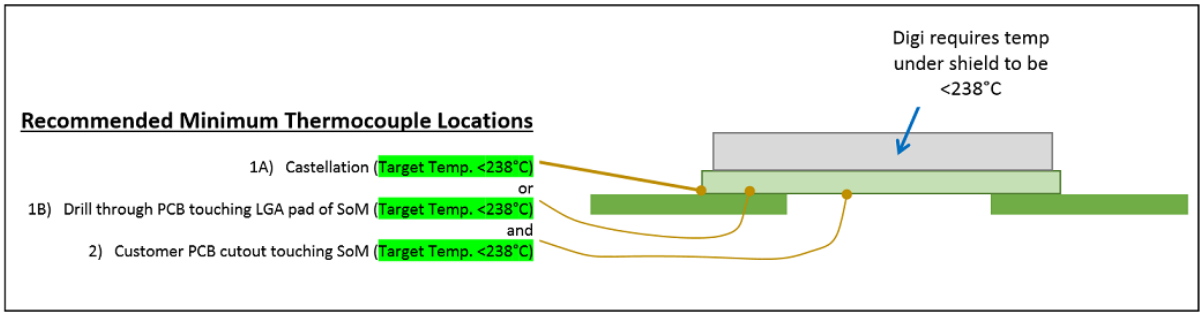
- Keep SoM below 238°C during the reflow cycle for castellation AND LGA applications.
- Time Above Liquidous (TAL) is recommended to be between 55 to 65 seconds.
- Use of 40AWG K-type thermocouple and M.O.L.E or equivalent thermal profiler is recommended.



Recommended reflow profile only - 10 heating zone convection reflow oven
Modifications to profile may be required to fit specific equipment, application, process or design

Two thermocouple locations are recommended to achieve proper attachment of SoM:

- For castellation applications, one thermocouple located on a castellation (preferable a power or ground castellation) and a second located near the underside center of the SOM to ensure SOM is not exposed to excessive temperatures.
- For LGA applications, one thermocouple located on the outer-most row (preferable a power or ground pad) and a second located near the underside center of the SOM to ensure SOM is not exposed to excessive temperatures.



Note Digi recommends X-ray analysis after reflow to confirm proper mounting and solder reflow.

The ConnectCore 91 is approved to withstand a total of four (4) reflow cycles. Two (2) reflow cycles are required for manufacturing the ConnectCore 91. Two (2) reflow cycles are remaining for mounting the module on the carrier board. Digi strongly recommends soldering the ConnectCore 91 during the last reflow cycles of the carrier board manufacturing process.